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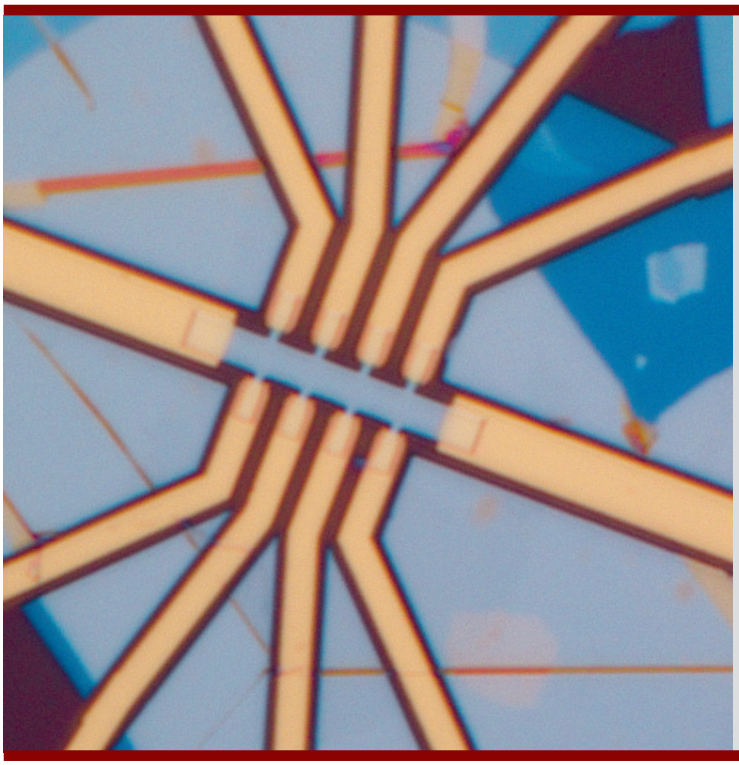
Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record



2D Material Device Architectures:

Process Optimisation and Characterisation

Lene Gammelgaard
PhD Thesis August 2016

DTU Nanotech
Department of Micro- and Nanotechnology

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Ph.D. Thesis

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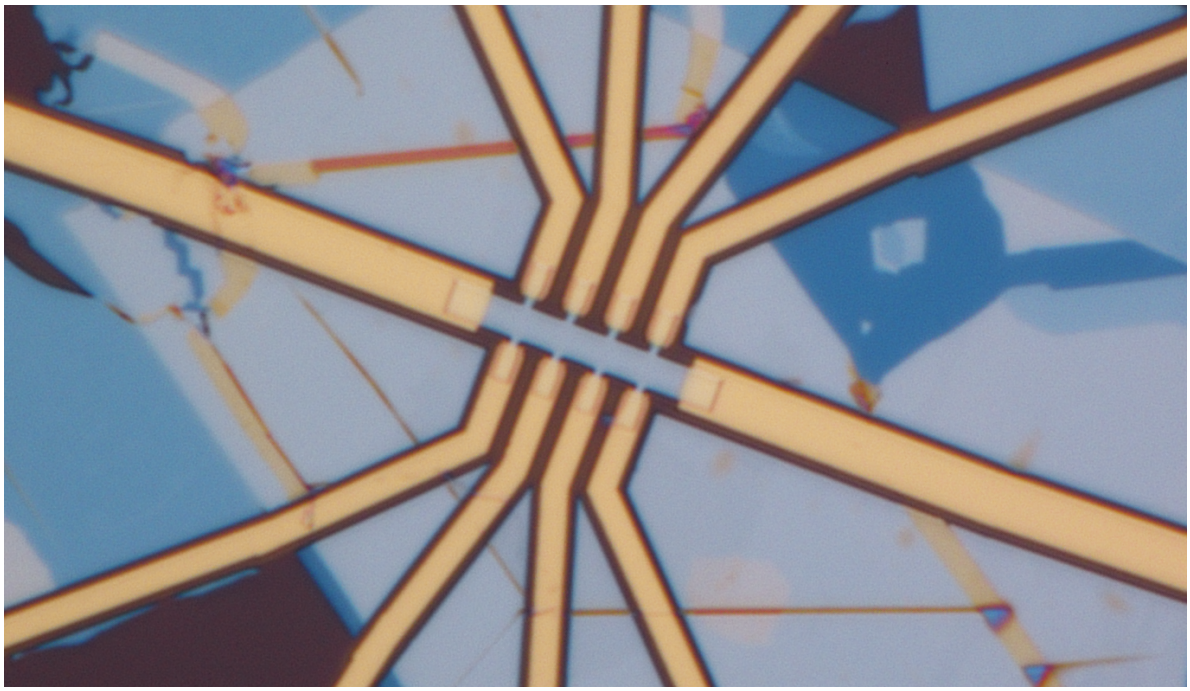

Supervisor: Professor Peter Bøggild
Co-supervisors: Associate Professor Timothy J. Booth and Professor Antti-Pekka Jauho

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August, 2016

Front page image: Optical micrograph of a van der Waals heterostructure of hexagonal boron nitride encapsulated graphene.

Abstract

A wide range of two-dimensional layered materials have been isolated and synthetically grown since the discovery of graphene. These layered materials can be thinned down to monolayer from their bulk crystals and re-stacked into arbitrary van der Waals heterostructures with atomic layer precision. The possible combinations of layers are nearly infinite, which leads to an extensive demand for robust and universal fabrication techniques and device architectures, that can enable the full potential of the extensive library of two-dimensional materials.

Recent experimental development has made it possible to stack two-dimensional crystals with atomically clean interphases, through a procedure termed van der Waals assembly. We have further developed this assembly method with the "Hot pick-up" method, which enables batch assembly as well as assembly with pre-patterned crystals. Inclusion of pre-patterned crystals increases the flexibility of device architectures significantly.

In this work, devices and experiments have been performed with graphene, semi-conducting transition metal dichalcogenides and hexagonal boron nitride. Two robust and reliable approaches have been used. Firstly, stencil lithography has been applied in particular for process optimisation and fault-finding. Stencil lithography has the advantage of being fast, cheap and clean, and has in this thesis been applied for fabrication of graphene and transition metal dichalcogenides devices. Secondly, van der Waals heterostructures have been fabricated with both graphene and transition metal dichalcogenides layers encapsulated in hexagonal boron nitride. Electrical contacts to encapsulated graphene have been developed to accommodate the requirement of field-effect gating by top- and back gates. Devices of mono-, bi- and trilayer graphene encapsulated in hexagonal boron nitride have been fabricated and studied electrically. These devices have field-effect mobilities comparable with the highest values reported. Furthermore, state of the art nano-patterns have been fabricated into encapsulated graphene. It was also explore how graphene layers perform as tunable contacts to transition metal dichalcogenides layers encapsulated in hexagonal boron nitride. This architecture yields high performance devices, where high mobilities of the air sensitive $MoTe_2$ crystals have measured, and metal-insulator transition have been observed in monolayer MoS_2 devices. Additionally, the long-term stability of transition metal dichalcogenides has been studied, and the order of the layers has been demonstrated detectable by atomic force microscopy.

The encapsulated van der Waals heterostructures give high performance and long-term stability of two-dimensional layered materials. The integration of pre-patterned layers, post-patterning of van der Waals heterostructures and detection of the layer order enables control – not only of the vertical ordering of atomic layers – but also in the lateral dimension, facilitating fabrication of advanced metamaterials and nano-devices with better or completely new functionalities.

Resumé

Siden opdagelsen af grafen, er en bred vifte af lagdelte todimensionelle krystaller blevet isoleret og groet syntetisk. Fra disse materialer kan enkeltlagskrystaller isoleres og gen-stables i van der Waals heterostrukturer med atomar lagpræcision. De mulige kombinationer af lag er næsten uendelige. Dette fører til en stor efterspørgsel af robust og universel fremstillingsteknikker og design, der kan bruges til at udforske det fulde potentiale af de mange todimensionelle krystaller.

Eksperimentel udvikling har for nyligt muliggjort gen-stabling af de todimensionelle krystaller ved hjælp af van der Waals kræfter og uden kontaminering mellem lagende. Vi har videreudviklet denne metode med "Hot pick-up" metoden, som gør batch fabrikering samt inkludering af pre-mønstrede krystaller muligt. Fleksibiliteten af design bliver betydelige øget med inkludering af de pre-mønstrede krystaller.

Todimensionelle krystaller af grafen, halvledende overgangsmetal dichalkogenider og hexagonal bornitrid er blevet brugt til eksperimenter i dette projekt. To fremgangsmåder er blevet benyttet. For det første er stencil litografi blevet anvendt til procesoptimering og fejlfinding. Fabrikation med stencil litografi har fordel af at være hurtig, billig og ren, og er blevet brugt til at elektriskkontakte både grafen og overgangsmetal dichalkogenider. For det andet er van der Waals heterostrukturer blevet fremstillet både med lag af grafen og lag af overgangsmetal dichalkogenider indkapslet i hexagonal bornitrid. Prøver med enkelt-, to- og trelags grafen krystaller indkapslet i hexagonal bornitrid er blevet fabrikeret og studeret elektrisk. Disse prøver har felteffekt mobiliteter som er sammenlignelige med de højeste værdier tidligere rapporteret. Desuden er nano-strukturer af exceptionel høj densitet blevet fremstillet i enkeltlags grafen krystaller også indkapslet i hexagonal bornitrid. Garfens evne som todimensionel-kontakter til overgangsmetal dichalkogenider indkapslet i hexagonal bornitrid er også blevet undersøgt. Høje mobilitet er blevet målt på luft-sensitive krystaller af $MoTe_2$, og metal-isolator-overgang er blevet observeret i en enkeltlags MoS_2 krystal. Derudover er stabilitet af overgangsmetal dichalkogenider blevet undersøgt, og rækkefølgen af lagene er blevet demonstreret påviselig ved brug af atomart kraftmikroskopi.

De indkapslede van der Waals heterostrukturer har høj ydeevne og stabilitet. Integration af pre-mønstrede lag, post-mønstering af van der Waals heterostrukturer, samt detektion af lagens rækkefølge giver stor kontrol og skaber muligheder for at fremstille avancerede metamaterialer og nano-enheder med bedre eller helt nye funktionaliteter.

Preface

This thesis has been carried out at the Department of Micro- and Nanotechnology at the Technical University of Denmark in the period from August 2013 to August 2016. The cleanroom facilities at DTU danchip and transmission electron microscopes at Center for Electron Nanoscopy have been used. The research was financed by internal founding and the EC Graphene FET Flagship, grant agreement number 604391. The main supervisor of this project has been Professor Peter Bøggild and the co-supervisors have been Associate Professor Timothy J. Booth and Professor Antti-Pekka Jauho.

First of all, I would like to thank my supervisor Professor Peter Bøggild for guidance, support and freedom to explore during my Ph.D. project. You have been a great source of inspiration and it has been exciting to be in the science "race" of the 2D materials with you and the rest of the group. I would also like to thank me co-supervisors Associate Professor Timothy J. Booth and Professor Antti-Pekka Jauho for guidance and advices.

I would like to thank all present and former members of the Nanocarbon group at DTU Nanotech; I have enjoyed working with you and I am looking forward start new exciting projects with you in the future. To mention a few I would like to thank; Joachim Dahl Thomasen and Patrick Rebsdorf Whelan for always being helpful and assisting with transmission electron microscopy characterisation, David M. A. Mackenzie and José M. Caridad for help with the low temperature measurement setups. I would also like to thank the former members; Dirch H. Petersen, Alberto Cagliani and Lisa Katharina Tschammer for our collaborations, guidance and productive discussions in the beginning of my Ph.D. project. To Filippo Pizzocchero and Bjarke Sørensen Jessen thanks for both introducing me to the vdW assembly method and for our teamwork in the vdW team. I believe that we achieved more together than we would have separately. Furthermore, I would like to give a special thanks to Bjarke Sørensen Jessen. Thanks for all the collaborations and discussions on fabrication, devices design and physics. Also, thanks for you enjoyable company during the long workdays in the office and laboratories, you made it all a lot more fun!

I would like to thank the staff at DTU Danchip, in particular Tine Greibe and Peixiong Shi for assistance with the electron beam system, and also Helle V. Jensen, Conny Hougaard, Mikkel Dysseholm Mar, Thomas Aarøe Anhøj and Henrik Nielsen, for help and guidance in the cleanroom. To Helene Koling, Astrid Lystbæk Andersen, Mikkel Settnes and in particular Marie Pødenphant Jensen I am very grateful for your help with proofreading of the thesis.

Finally, I would like to thank my family and friends for always supporting me. A great thank goes to my parents for housing me while I was writing the thesis, you made the long days of writing far more delightful.

Lene Gammelgaard
Technical University of Denmark
Kgs. Lyngby, August 14st, 2016

Acronyms

0D zero-dimensional

1D one-dimensional

2D two-dimensional

2DEG two-dimensional electron gas

3D three-dimensional

AFM atomic force microscope/microscopy

Ar argon

Au gold

BN boron nitride

CAB cellulose acetate butyrate

CNP charge neutrality point

Cr chromium

CVD chemical vapour deposition

E-Beam electron beam

EBL electron beam lithography

FIB focused ion beam

FWHM full width at half maximum

GAL graphene antidot lattice

hBN hexagonal boron nitride

IPA isopropyl alcohol

LHS left hand side

mfp mean free path

MIBK methyl isobutyl ketone

MoS_2 molybdenum disulfide

$MoSe_2$ molybdenum diselenide

$MoTe_2$ molybdenum ditelluride

O_2 diatomic oxygen

Pd palladium

PDMS polydimethylsiloxane

PMMA polymethyl methacrylat

PPC polypropylene carbonate

RHS right hand side

rpm revolutions per minute

RT room temperature

sccm standard cubic centimeters per minute

SEM scanning electron microscope/microscopy

SF_6 sulfur hexafluoride

Si silicon

SiO_2 silicon dioxide

TEM transmission electron microscope/microscopy

Ti titanium

TLM transfer length measurement

TMD(s) transition metal dichalcogenide(s)

vdP van der Pauw

vdW van der Waals

WS_2 tungsten disulfide

WSe_2 tungsten diselenide

Contents

1 Introduction

1.1 Background

Experimental research with two-dimensional (2D) layered materials is a relatively young field, but it has never the less developed rapidly over the last decade. Graphene was first isolated from graphite and electrically characterised in 2004 by A. K. Geim and K. Novoselov at the University of Manchester [1]. In 2010 they were awarded with the Nobel price in physics "for groundbreaking experiments regarding the two-dimensional material graphene". Graphene crystals were first isolated (mechanical exfoliation) from bulk graphite with something as simple as tape [2]. Mechanical exfoliation is performed by applying and releasing tape with flakes of graphite on a clean substrate of silicon with a layer of thermally grown oxide, on which the graphene crystals can be identified by their contrast. Graphene has since been isolated by liquid-phase exfoliation [3] and grown in large areas using chemical vapour deposition (CVD) [4].

A wide range of other 2D layered materials with various properties have obtained great attention since graphene was isolated. Among these materials are black phosphorus, transition metal dichalcogenides, hexagonal boron nitride, all of which can be mechanically exfoliated from either naturally occurring or artificially synthesised bulk crystals. The layers of 2D crystals are one to a few atoms thick and are held together in their 2D lattice by strong covalent bonds and by van der Waals (vdW) interaction in-between the layers. The flakes have a wide range of properties, which may be altered by re-stacking the crystals into so called vdW heterostructures.

Graphene

All carbon materials are available in multiple atomic structures; there are three-dimensional (3D) graphite, diamond and amorphous carbon, one-dimensional (1D) carbon nano tubes and the zero-dimensional (0D) fullerene, see Fig. 1.1. Graphene consists of carbon atoms in a flat hexagonal Bravais lattice. The lattice is only one atom thick, but exfoliated flakes may be hundredths of micro meters in their lateral dimensions, making the crystal as close to 2D as possible.

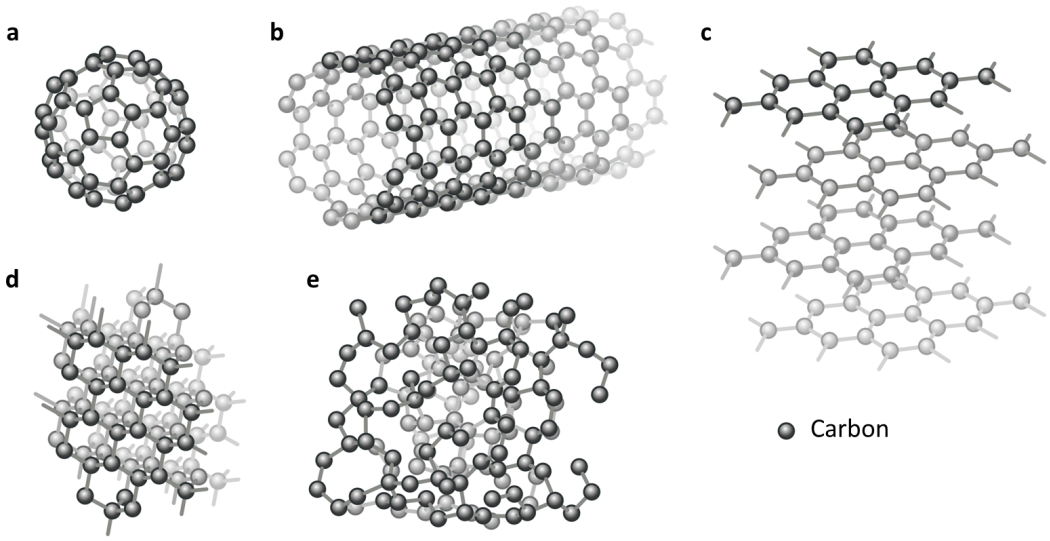


Figure 1.1: *Balls and sticks models of the structure of various all carbon based materials: (**a**) Zero-dimensional fullerene, (**b**) one-dimensional carbon nanotube, (**c**) the layered structure of graphite, of which one layer is the two-dimensional graphene. Three-dimensional structures of (**d**) diamond and (**e**) amorphous carbon. Adapted from [5].*

Graphene has many outstanding properties. It is the mechanically strongest material ever measured [6], it is the best material at conducting heat [7] and it has an exceptional high mobility [8]. One of the remarkable qualities of graphene is its unique electronic band structure. The carbon atom has four valence orbitals. Three of them, the s-, p_x- and p_y-orbitals, are combined to form sp^2 hybridised orbitals, which form three equally spaced covalent bonds in the graphene lattice. The electrons in the last orbital, the p_z-orbital, are named π electrons, they are located above and below the graphene sheet and are highly mobile.

The dispersion relation of the π-bands may be calculated with a tight-binding model including nearest- and next nearest-neighbour hopping. The π and π^* bands meet in discrete points, the Dirac points, making graphene a semi-metal or zero-gap semiconductor, see Fig. 1.2. Only a small energy range around the Dirac point is probed in normal transport measurements, and

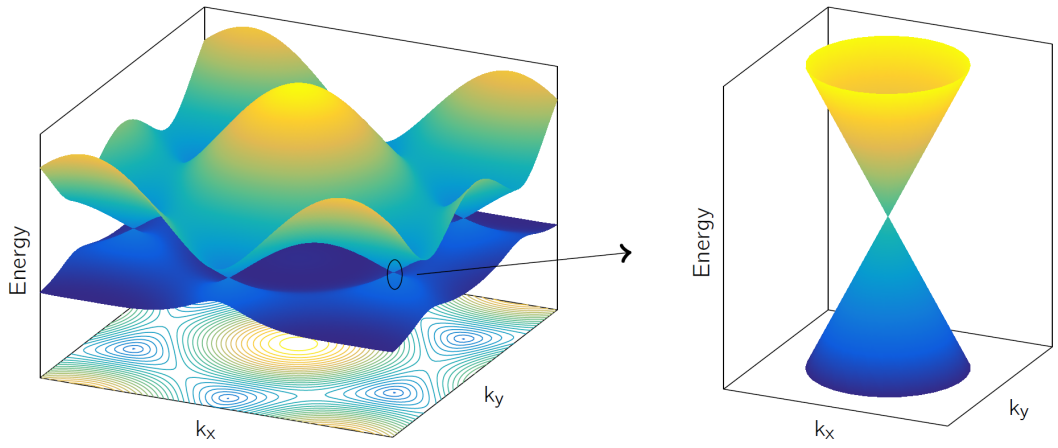


Figure 1.2: *Electronic dispersion relation of monolayer graphene. The conduction and valence bands touch in six discrete Dirac points at the vertices of the hexagonal Brillouin zone. The zoom-in shows the linear behaviour close to the Dirac point.*

the full dispersion relation expanded around the Dirac point yields the following linear relation

$$E_{\pm}(\mathbf{q}) \approx \pm\hbar v_F|\mathbf{q}| \ , \tag{1.1}$$

where $\hbar$ is Planck's constant, and $\mathbf{q}$ is the wavevector measured Dirac point. The Fermi velocity $v_F \approx 10^6$ m/s is ~ 300 times smaller than the speed of light, making it possible to explore the physics of relativistic particles.

Bi- and trilayer graphene are Bernal-stacked (AB-stacked). Half of the atoms of the second layer will be above the center of a hexagon in the first layer, and the other half will be directly above an atom in the first layer. The stacking arrangement is important for the properties, two randomly (not Bernal-stacked) stacked monolayer graphene will not behave as bilayer graphene but rather as two monolayer crystals [9]. The properties of multilayer graphene flakes are radically different from those of monolayers of graphene. For instance, bilayer graphene has a zero band gap as monolayer graphene has, but a parabolic band structures. Furthermore, a non-zero band gap is induced when bilayer graphene is under the influence of an electrical field [10].

Hexagonal Boron Nitride

Boron nitride (BN) can, as the family of carbon based materials, exist in various structures, 3D cubic BN, 2D hexagonal BN, and 1D BN nanotubes. The crystal structure of hexagonal boron nitride (hBN) is similar to that of graphene, boron and nitride atoms sit in a hexagonal lattice each occupying one of the two sub-lattices in its unit cell, see illustration in Fig. 1.3a. In contrast to graphene, the layers in hBN are stacked in an AA' fashion where a boron (nitride) atom in the lattice will be above the nitride (boron) atom of the underlying layer [11]. Furthermore, hBN is a wide band-gap semiconductor as a result of the two atoms in the unit cell. The band gap of hBN is in the order of 5.2 eV-5.9 eV [12].

Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDs) are 2D layered crystals with the chemical formula MX_2. In the lattice, atoms of transition metal such as molybdenum, tungsten and hafnium, are located in-between two chalcogen such as sulfur, selenium and tellurium, see illustration of MoS_2 in Fig. 1.3b. There are hundredths of combinations of transition metal and chalcogen [15] leading to a wide range of direct- and indirect-band-gap semiconductors, ferromagnetic and nonmagnetic metal crystals [16]. The band gaps of the TMDs are mainly in the range of 1 eV to 2 eV [15, 17, 18], and the band structure of the TMDs changes with variation in number of layers. Many of the TMDs undergo a transition from an indirect to a direct band

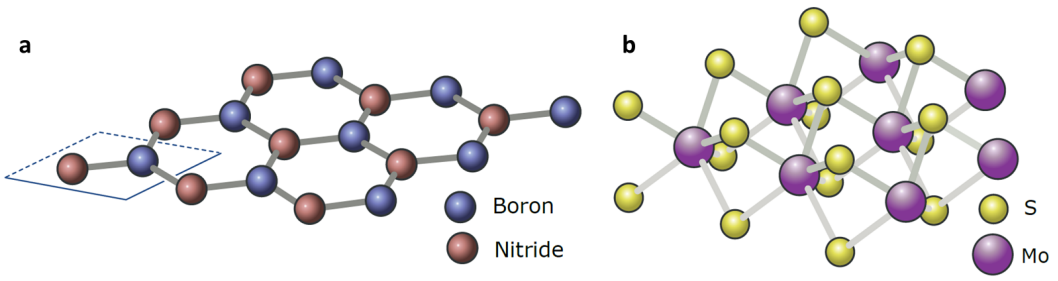


Figure 1.3: *Balls and sticks models of the crystal structure of (**a**) hexagonal boron nitride (hBN) and (**b**) the transition metal dichalcogenide molybdenum disulfide, MoS_2. The unit cell of hBN is indicated by the rhombus in (**a**). Adapted from [13, 14].*

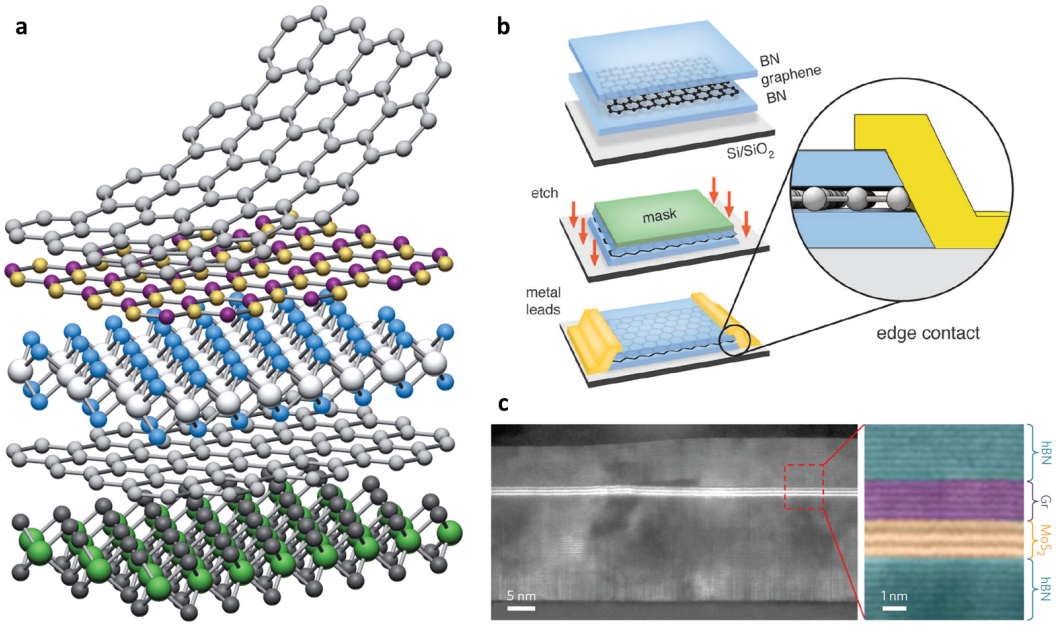


Figure 1.4: *(**a**) Illustration of van der Waals heterostructure of monolayer crystals. (**b**) Schematic of the fabrication of 1D edge contacts to hBN-encapsulated graphene. (**c**) Cross-sectional transmission electron micrograph of intermediate contact of multilayer graphene to trilayer MoS_2 in a hBN-encapsulated device. Adapted from [21, 22, 23].*

gap when thinned down to monolayer due to quantum-mechanical confinement. For instance, monolayer MoS_2 has a direct band gap of about 1.8 eV at the K point of the Brillouin zone, while bilayer to bulk MoS_2 have an indirect band gap. The band gap of bulk MoS_2 is 1.2 eV [19]. The most frequently studied semiconducting TMDs are MoS_2, $MoSe_2$, $MoTe_2$, WS_2 and WSe_2.

There excites hundreds of 2D layered materials, and the crystals can be re-stacked to create an endless number of vdW heterostructures. In this thesis 2D crystals of graphene, hBN and the three TMDs; MoS_2, $MoTe_2$ and WSe_2 have been the main crystals used for device fabrication and experiments.

van der Waals Heterostructures

"What could we do with layered structures with just the right layers? What would the properties of materials be if we could really arrange the atoms the way we want them?" From Richard P. Feynman, "There's Plenty of Room at the Bottom" 1959.

Over half a century later researchers are working intensively on these two questions, as we now are capable of arranging down to monolayers of 2D crystals into arbitrary vdW heterostructures, see illustration in Fi. 1.4a. Not only can the arrangement of the layers be designed but the layers can also be pre-patterned before stacking [20] and stacked with atomically clean inter-phases [21]. The technique to make these structures is named vdW assembly, as the vdW interaction between the atomically flat layers is employed.

Flakes of hBN are very applicable in vdW heterostructures, both as substrate [24], for full encapsulation, shielding the crystals from the environment [21] and as vertical tunnel barrier [25]. One of the great advantages of using hBN compared to SiO_2 as a substrate is that it is atomically flat, free of dangling bonds and the surface phonon energies in hBN do not limit

the transport in graphene at room temperature as for SiO_2.

There is a lattice mismatch between the graphene and the hBN lattice, as the bond length of the covalent B-N bonds in hBN are approximately 1.8 % larger than that of covalent C-C bonds in graphene [26]. This lattice mismatch leads to the formation of a moiré pattern when graphene is placed on hBN. The size of the moiré wavelength (period) depends on the rotational alignment, angle, between the hBN and graphene lattice, the smaller angles leading to the longest wavelengths, with a 14 nm period for graphene perfectly aligned to the hBN. The moiré super lattice leads to formation of so called moiré minibands in the graphene band structure, and will at small angles open a band gap at the charge neutrality point of the graphene [27].

Full encapsulation with hBN creates the challenge of contacting the graphene with metal leads. This challenge was elegantly solved by fabricating 1D contacts to the edge of the hBN-encapsulated graphene [21]. Fabrication of 1D edge contacts is illustrated in Fig. 1.4b. Unfortunately the 1D edge contacts have not yet been shown to work for TMDs, but graphene can be used as intermediate contact to TMDs within the stacks [23]. Cross sectional transmission electron micrograph of an intermediate contact of multilayer graphene to trilayer MoS_2 is seen in Fig. 1.4c.

Crystals can in principle be re-stacked in any order in vdW heterostructures giving rise to an infinite amount of artificial materials. Hence there are a wide range of materials to be studied and exploited.

1.2 Scope of This Thesis

The overall goal in this thesis is to develop flexible architectures and robust fabrication techniques for high yield, high quality and long-term stability of 2D devices, including:

1. **Methods for clean and fast testing**
   2D materials are highly influenced by the surroundings – need clean methods of electrical contacting and characterisation for process optimisation.
2. **State of art performance for basic and applied research**
   vdW heterostructures of exfoliated crystals give the highest possible performance and are therefore needed for prototyping – need to test theoretical predictions and application-related limit (i.e. max speed of transistors, max efficiency of solar cells) before moving to large-scale fabrication.
3. **Simplify and streamline van der Waals assembly**
   Still in literature advanced structures are tedious and complicated to make – need cheap, fast, accessible and reliable protocols to make vdW assembly available to a much larger community.
4. **Methods for systematic screening of hBN-encapsulated 2D materials**
   There are hundreds of 2D materials and therefore a great demand for effective, reliable, high quality prototyping, not only to test individual 2D material but also to test the infinite number of crystal combinations in vdW heterostructures.
5. **Enable integration of patterned layers in vdW heterostructures**
   The vdW assembly yields complete control of the layer sequences – integration of pre-patterned layers and patterning of layers within stacks give control in the lateral dimension too. Patterning of 2D materials gives rise to intriguing possibilities for both controlling and manipulating electronic, plasmonic and photonic properties, creating unique materials.

6. **Pave the way for large-scale fabrication**
   The vdW assembly provides the test platform for screening the numerous possible device architectures, but the fabrication processes (i.e. etching and contacts) will be applicable for large-scale fabrication with CVD grown crystals.

1.3 Thesis Outline

An introduction to the family of 2D crystals and vdW heterostructures has been given together with the scope of this thesis. Listed below is a brief summary of the chapters of the thesis as a guide to the reader.

Chapter 2 presents the basic concepts of electronic transport in 2D systems with emphasis on transport in graphene. Scattering mechanisms' effect on the transport is outlined, as the all surface 2D crystals are highly affected by the surroundings. Furthermore, a section is dedicated to contacts, the principles of ohmic and Schottky contacts are presented together with the intermediate graphene to TMD contacts, which are used for contacting hBN-encapsulated TMDs. Finally, the techniques used for two- and four-terminal field-effect measurements are described, and a short introduction to the experimental setups is given.

Chapter 3 gives a short introduction to the characterisation tools used for inspection and characterisation of 2D crystals and devices. The tools include; optical microscopy, Raman spectroscopy, atomic force microscopy, scanning and transmission electron microscopy.

Chapter 4 explains the fabrication techniques and processes used to go from bulk crystals to electrically contacted 2D devices. All device fabrication start with mechanical exfoliation of crystals and this will therefore be described. Exfoliated flakes can either be processed directly into devices or made into heterostructure. The "Hot pick-up" technique for van der Waals heterostructure assembly is carefully described step by step. Fabrication processes used for etching the 2D flakes/heterostructures into desired shapes and electrically contacting are outlined. Finally, three design variations of the 1D edge contacts to hBN-encapsulated graphene are introduced, among these contacts have one type been developed for top gating, and one for back-gating with graphite in all 2D crystal devices.

Chapter 5 presents the results gained with graphene devices. Clean graphene stencil devices have been used for process optimisation and testing, results from these are first presented. Then the results from heterostructures of hBN-encapsulated mono-, bi- and trilayer graphene assembled by the "Hot pick-up" method are given. Finally, preliminary results from hBN-encapsulated and dense nano-patterned graphene are presented with details on the process optimisation.

Chapter 6 presents the results related to work with transition metal dichalcogenides. The stability of TMD flakes and particularly edges of flakes has been examined by atomic force microscopy. Furthermore, the electrical stability of WSe_2 stencil devices on SiO_2 has been studied, and result from these are presented here. Finally, results from low temperature electrical characterisation of vdW heterostructures of hBN-encapsulated TMDs with graphene intermediate contacts are presented.

Chapter 7 gives an overall conclusion of the thesis and an outlook.

2 Electronic Transport

This chapter focuses on the electronic transport in 2D systems. The concepts of diffusive and ballistic transport are outlined, as well as how the scattering mechanisms in 2D systems affect the transport. Furthermore, a section is dedicated to contacts and contact resistance, introducing the graphene to TMD contacts. Finally, the specific details on execution of two- and four-terminal measurements are given together with a short description of the experimental setups used in this work.

Contents

2.1 Electrical Field-Effect, Mobility and Mean Free Path

An external gate is in field-effect measurements used to charge the number of charge carriers in the device channel while measuring the resistance/conductance of the channel. The device mobility and mean free path can then be estimated from these measurements. Mainly back-gates of highly doped silicon are used, but devices with graphite top- and back-gates have also

been fabricated, with hBN flakes as the dielectric separating the gate and the device channel. Devices are fabricated on low resistivity ($1 - 2\,\mathrm{m\Omega \cdot cm}$) silicon wafers with a layer of thermally grown silicon dioxide as the dielectric. The number of charge carriers induced in the device channel is described as

$$n = \frac{CV_g}{e} + n_Q \left[1 - \sqrt{1 + \frac{CV_g}{en_Q}} \right] , \tag{2.1}$$

$$n_Q \equiv \frac{\pi}{2} \left(\frac{C\hbar v_F}{e^2} \right)^2 , \tag{2.2}$$

where C is the capacitance per area, V_g is the applied gate voltage, e is the elementary charge. . where $\hbar$ is Plank's constant and v_F is the Fermi velocity. The second term of the right hand side of Eq. (2.1) is the quantum capacitance, which is neglectable for the gate dielectric thicknesses used here, and the gate induced charge carriers becomes

$$n \approx \frac{CV_g}{e} = \frac{\varepsilon_0 \varepsilon_r}{d} \frac{V_g}{e} . \tag{2.3}$$

The capacitance is similar to a parallel plate capacitor, $C = \varepsilon_0 \varepsilon_r / d$, where ε_0 is the vacuum permittivity, ε_r is the relative permittivity and d is the thickness of the dielectric. If more than one dielectric material separates the device channel from the gate the total capacitance is calculated as for two capacitors in series. This is the case for hBN-encapsulated devices where both a SiO_2 layer and a hBN flake separate the device channel form the silicon back-gate, $C_{tot}^{-1} = C_{SiO2}^{-1} + C_{hBN}^{-1}$.

The resistance, R, and conductance, G, of the device channel are measured during a field effect measurement. This measurement is done by applying a constant bias voltage, V, across the channel and measuring the current, I, or vice versa. The resistance as a function of the applied gate voltage is then found from Ohm's low, which gives the relation:

$$R = \frac{1}{G} = \frac{V}{I} . \tag{2.4}$$

The resistance/conductance of the device channel will depend on the dimensions of the channel, and the material parameters resistivity, ρ, and conductivity, σ, with the relation $\rho = 1/\sigma$, are therefore introduced. The resistance and resistivity in 2D and 3D are related as

$$R = \rho \frac{L}{A} \ (3D) ,$$
$$R = \rho \frac{L}{w} \ (2D) .$$

Here, L is the length of the channel, A is the cross-sectional area of a thick channel, and w is the width of the channel. Details regarding techniques used for electrical measurements are outlined later in this chapter in Sec. 2.4. In the following, the diffusive and ballistic transport regimes are reviewed.

2.1.1 Diffusive Transport

The Drude model treats the transport of the charge carriers in a solid classically. When charge carriers move along a material under a constant electrical field they collide with randomly distributed scattering centres making the transport diffusive. In the Drude model, the collisions are elastic, and the carriers move ballistically in-between scattering events. The mean free path (also called momentum relaxation length), λ_{mfp}, is the mean distance travelled, along the

transport direction, by the electron/hole between two collisions. The mean free path is given as

$$\lambda_{mfp} = v_F \tau \ , \tag{2.5}$$

where τ is the collision time (or relaxation time) an electron/hole has travelled since the last collision. The Fermi velocity and collision time are given by

$$v_F = \frac{\hbar k_F}{m^*} \ ,$$
$$\tau = \frac{m^* \mu}{e} \ ,$$

where m^* is the effective mass of the charge carriers and μ is the mobility, e is the elementary charge and k_F is the Fermi wavevector. The Fermi wavevector for all 2D systems is given by

$$k_F = \sqrt{\frac{4\pi n}{g_s g_v}} \ , \tag{2.6}$$

where g_s and g_v are the spin and valley degeneracy. For monolayer graphene $g_s g_v = 4$, whereas $g_s g_v = 2$ for bilayer and thicker graphene flakes as well as 2D electron gases (2DEG) in general [28]. The field-effect mobility, μ, describes how well the charge carriers move through a material while under an electrical field, $v_d = \mu E$, where v_d is the drift velocity and E is the electrical field strength. The conductivity and the field-effect mobility for diffusive Drude-typed transport are linked as follows

$$\sigma = en\mu \ . \tag{2.7}$$

Here, n is the induced charge carriers, which can be calculated from the applied gate voltage via Eq. (2.3). The conductivity is calculated from the device dimensions, the voltage drop across the channel and current in the channel, $\sigma = \frac{I}{V}\frac{L}{w}$.

2.1.2 Ballistic Transport

Ballistic transport occurs when the motion of the charge carriers through the sample is without collisions except for specular reflections from device boundaries. If the mean free path is much larger than the device dimension, or the device dimensions are made smaller than λ_{mfp} the transport is considered ballistic, $w, L < \lambda_{mfp}$. An intermediate regime, the quasi-ballistic regime is defining when $w < \lambda_{mfp} < L$, [30]. Illustrations of scattering in diffusive, quasi-ballistic and ballistic device channels are seen in Fig. 2.1.

For ballistic transport the conductivity does not exist as a local device property, as the measured conductance will depend on the ballistic pathways/trajectories between contacts and boundaries of the structure. The conductance of the device may be described by the Landau formula

$$G = g_0 \sum_n T_n \ , \tag{2.8}$$

where T_n is the transmission probability for the n'th channel, $g_0 = 4e^2/h$ for monolayer graphene, the factor of 4 accounts for the spin and valley degeneracy $g_s g_v = 4$. If perfect transmission is assumed for monolayer graphene the ballistic conductance of the device will be given by [31]

$$G_{bal}(n) = \frac{4e^2}{h} N = \frac{4e^2}{h} \frac{w\sqrt{\pi n}}{\pi} \ .$$

$N = wk_F/\pi$ denotes the number of longitudinal modes in a channel of width w, and k_F is the Fermi wavevector, see Eq. (2.6). Conductance measurements of devices where the propagation of the charge carrier is ballistic will therefore have a square root dependency on the induced charge carriers, $G_{bal}(n) \propto \sqrt{n}$.

2.2 Scattering Processes

This section deals with the scattering mechanisms affecting the transport in 2D material. The measured quantities will be a result of the scattering sources in the system. The influence of the various scattering lengths of the system are approximated by Matthiessen's rule

$$\frac{1}{\lambda_{mfp}} = \frac{1}{\lambda_{LA}} + \frac{1}{\lambda_{ph}} + \frac{1}{\lambda_C} + \frac{1}{\lambda_{sr}} + \frac{1}{\lambda_{boundary}} + ... \tag{2.9}$$

The rule can also be expressed in terms of the collision time or the mobility

$$\frac{1}{\tau} = \frac{1}{\tau_{LA}} + \frac{1}{\tau_{ph}} + \frac{1}{\tau_C} + \frac{1}{\tau_{sr}} + \frac{1}{\tau_{boundary}} + ...$$
$$\frac{1}{\mu} = \frac{1}{\mu_{LA}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_C} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_{boundary}} + ...$$

The subscripts refer to the scattering mechanism related to the parameter, which will be outline in the following. LA relate to scattering with intrinsic longitudinal acoustic phonons in the crystal, and ph are scattering with remote phonons in the substrate. C and sr refers to Coulomb (long-range) and short-range scattering, and finally scattering on boundaries of the device.

2.2.1 Intrinsic Longitudinal Acoustic Phonons in Graphene

Electron-phonon interaction between the charge carriers and the longitudinal acoustic phonons, LA, of the graphene lattice causes scattering. The resistivity contribution due to LA phonons has the following linear dependency with temperature [8, 32]

$$\rho_{LA}(T) = \frac{h}{e^2}\frac{\pi^2 D_A^2 k_B}{2h^2\rho_s v_s^2 v_F^2}T \ ,$$

where k_B is Botzmanns constant, $\rho_s = 7.6 \cdot 10^{-7}\,\mathrm{kg/m^2}$ is the two-dimensional mass density of graphene, $v_F = 10^6\,\mathrm{m/s}$ is the Fermi velocity and $v_s = 2.1 \cdot 10^4\,\mathrm{m/s}$ is the velocity of sound

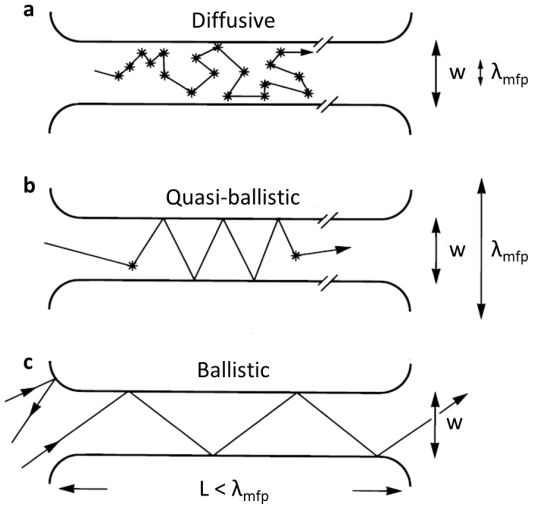


Figure 2.1: *Trajectories of charge carriers in a device channel. (**a**) Schematic of diffusive transport, $\lambda_{mfp} < w, L$, scattering i (**b**) Quasi-ballistic regime $w < \lambda_{mfp} < L$, scattering occurs both at the boundary and at scattering centres in the device channel. (**c**) Ballistic regime where $w, L < \lambda_{mfp}$. Adapted from [29]*

in graphene. D_A the acoustic deformation potential which value is debated, values of 18 eV and 29 eV have been reported for SiO_2 supported graphene [8] and suspended graphene [31], respectively. On the other hand, a intrinsic acoustic deformation potential of 6.8 eV have been calculated theoretically [33], a smaller deformation potential will lead to a lower resistivity and thus a higher possible mobility.

For a deformation potential of 18 eV, the sheet resistivity due to LA phonons within the graphene is, at room temperature, approximately 30 Ω corresponding to a mobility of 200,000 cm^2/Vs at a charge carrier density of n = 10^{12} cm^{-2}. For D_A = 6.8 eV this mobility limit is approximately seven times higher. The resistivity due to the LA phonons decrease as the temperature is decreased, $\rho_{LA}(T) \propto T$. The acoustic phonon-limited mobility is therefore increasing when the temperature is lowered, as plotted in Fig. 2.2 for a deformation potential of 18 eV and 6.8 eV.

The phonon limited mobility due to acoustic phonon scattering is remarkable smaller for TMDs. At room temperature the mobility limits for monolayer MoS_2, $MoTe_2$ and WSe_2 is $\sim 400\ cm^2/Vs$, $\sim$2,500 cm^2/Vs and $\sim 700\ cm^2/Vs$, respectively [34, 35].

2.2.2 Extrinsic Surface Phonon Modes Effect on Graphene

Optical surface phonon modes in the substrate below the graphene flake may also lead to scattering. In general, surface phonon modes with energies of 50 meV to 200 meV lead to long-range electrical fields and thereby scattering. The scattering with surface phonon modes depends both on the temperature and the charge carriers density, n, [8]

$$\rho_{ph}(n,T) = B_1 n^{-\alpha} \left(\frac{1}{e^{(\hbar\omega_{s1}/k_B T)-1}} + \frac{6.5}{e^{(\hbar\omega_{s2}/k_B T)-1}} \right) .$$

Here, B_1 and α are fitting parameters, and $\hbar\omega$ is the energy of the phonon modes. SiO_2 have two strong surface optical phonon modes at energies of $\hbar\omega_{s1} \approx 59$ meV and $\hbar\omega_{s2} \approx 155$ meV [36]. On the other hand, the 2D crystal hBN, which may also be used as a substrate for graphene, has two modes of $\hbar\omega_{s1} \approx 97$ meV and $\hbar\omega_{s2} \approx 188$ meV [37]. It is clear that hBN is a favourable substrate for graphene, as the surface phonon modes of hBN do not limit the mobility. The room temperature resistivity induced by the surface phonon modes of hBN is approximately an order of magnitude smaller, $\sim 3\ \Omega$ [36], than that of the intrinsic LA phonon scattering. Contrary to the remote phonon modes of SiO_2, which limit the room temperature mobility of graphene to 40,000 cm^2/Vs. The optical surface phonon modes of SiO_2 dominates the scattering at high temperatures, above $\sim$ 165 K, as seen by the crossover of the LA and SiO_2 surface phonon line in Fig. 2.2.

2.2.3 Short-Range Scattering

Short-range scattering occurs at non-charged scattering centres such as lattice defects. The scattering interaction region is on the order of the carbon-carbon bond length.For monolayer graphene the mobility limited by short range scattering is inversely proportional to the carrier density, $\mu_{sr}^{Mono} \propto 1/n$ [38]. The collision time have a square root dependency and the conductivity related to the short-range scattering is constant with aspect to n as well as T ($\tau_{sr}^{Mono} \propto 1/\sqrt{n}$ and $\sigma_{sr}^{Monu} \propto C$). On the contrary, for multilayer graphene the mobility limited by short-range scattering is constant, $\mu_{sr}^{Multi} \propto C$, and $\sigma_{sr}^{Multi} \propto n$.

2.2.4 Long-Range Scattering

A charged scattering centre has a long-range Coulomb potential, on which the charge carriers can scatter. This scattering mechanism is named long-range or Coulomb scattering, and is

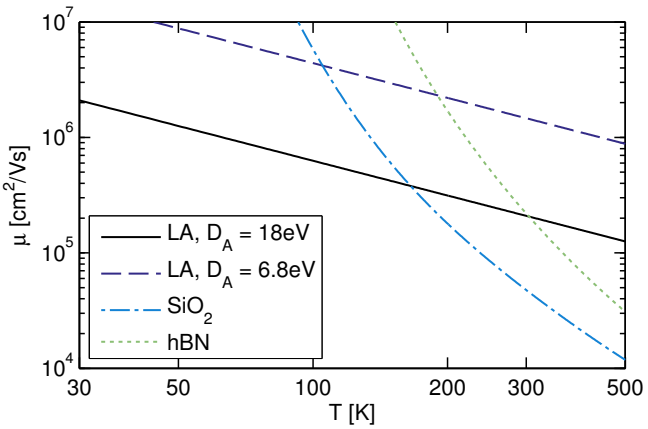


Figure 2.2: *Temperature dependency of the mobility of monolayer graphene limited by intrinsic longitudinal acoustic phonons, LA, plotted for a deformation potential of 18 eV and 6.8 eV, and mobility limited by extrinsic phonons from either a SiO_2 or a hBN substrate. Parameters for the plot are taken from [8], and $n = 10^{12}\,cm^{-2}$.*

one of the most common limiting mechanisms for transport in graphene devices on SiO_2. Trapped charges in the SiO_2 substrate, charged molecules or atoms close to the graphene and topographical variations all lead to Coulomb scattering.

Dielectrics materials with a high relative permittivity, ε_r, are favourable [39] as the magnitude of the electrical field from a point charge defect in the dielectric scales inversely with the absolute permittivity, through Coulomb's law

$$|E| = \frac{1}{4\pi\varepsilon_r\varepsilon_0}\frac{|q|}{r^2} \ .$$

Here, E is the electrical field from a point charge q in the distance r, and ε_0 is the vacuum permittivity. Coulomb scattering in graphene is therefore minimised when supported by a dielectric with a high dielectric constant, assuming that the density of charge defects are equal in the dielectrics. SiO_2 and hBN flaks are the main substrates used for devices here, and have relative permittivities of $\varepsilon_r^{hBN} = 5.09$ [40] and $\varepsilon_r^{SiO2} = 3.9$. Furthermore, point charges may also be screened by a nearby gate. It is possible to fabricate devices with very thin gate dielectric by using a graphite flake as a back-gate electrode and a thin hBN flake as the dielectric between the gate and the channel [27, 41].

In monolayer graphene the mobility limited by Coulomb scattering is independent of the carrier density, $\mu_C^{Mono} \propto C$, whereas for multilayer graphene the scaling is proportional to the carrier density, $\mu_C^{Multi} \propto n$ [38, 42]. The collision time and conductivity have the following dependencies for Coulomb scattering in monolayer graphene; $\tau_C^{Mono} \propto \sqrt{n}$ and $\sigma_C^{Mono} \propto n$.

The scattering length for short-range, $\lambda_{sr}^{Mono} \propto \tau_{sr}^{Mono} \propto 1/\sqrt{n}$, increases, whereas the scattering length for Coulomb scattering, $\lambda_C^{Mono} \propto \tau_C^{Mono} \propto \sqrt{n}$, decreases as the carrier density is lowered. According to Matthiessen's rule, Eq. (2.9), Coulomb scatting will therefore dominate the transport close to the Dirac point [43].

The Boltzmann formalism includes both the long-range and short-range scattering. The conductivity formula [28]

$$\sigma = \frac{e^2 v_F^2}{2} D(E_F)\tau \ ,$$

where $D(E_F)$ is the density of states at the Fermi energy. $D(E)$ for monolayer graphene and a multilayer graphene/2DEG are listed in Table. 2.1.

Table 2.1: *Electronic quantities and scattering dependencies for graphene and 2DEG.*

Parameter	**Graphene**	**2DEG**
Dispersion relation	Linear	Parabolic
Fermi energy, E_F	$\hbar v_F k_F$	$\frac{\hbar^2}{2m}k_F^2$
Density of states, $D(E)$	$\frac{g_s g_v E}{2\pi(\hbar v_F)^2}$	$\frac{g_s g_v m}{2\pi\hbar^2}$

2.2.5 SiO_2 versus hBN as a Substrate

To some extent monolayer graphene is like a cling-film; it conforms to the substrate. SiO_2 is not atomically flat and graphene supported by SiO_2 will therefore have corrugations similar to that of the SiO_2 surface [44, 45, 46]. Graphene on hBN, on the other hand, will be less corrugated, as in particular multilayer hBN flakes are atomically flat [24]. SiO_2 is a 3D crystal and will therefore have dangling bonds at the surface, this lead to a great amount of silanol groups (≡Si-OH) on the surface. These are polarised and will attract water and other polar molecules. Hence, water and other hydrocarbons may easily get trapped in-between the graphene and the SiO_2. For the 2D hBN flakes the picture is different, hBN is relatively inert and free of dangling bonds and surface charge traps [37, 47].

Corrugations are unwanted for several reasons. First of all the corrugations change the angle between the p_z-orbitals leading to local variations of the Dirac point [48]. Corrugations are therefore causing fluctuations in the Fermi level leading to formation of electron-hole puddles at the charge neutrality point [49]. Furthermore, the local curvature of the graphene increases its reactivity towards oxygen molecules [50], which together with H_2O molecules is known to lead to strong hole doping of graphene [50, 51, 52].

The temperature dependency at the minimum conductance is normally weak for devices of monolayer graphene on SiO_2. This weak dependency is attributed to the electron-hole puddles, as a temperature dependency is expected if $k_B T > E_{puddle}$. For graphene monolayers [31]

$$E_{puddle} \approx \hbar v_F \sqrt{\pi \tilde{n}} \ ,$$

where $\tilde{n}$ is the residual density considering electron-hole puddles. A typical value of the residual density is $\tilde{n} \approx 10^{11}\ \mathrm{cm}^{-2}$ for graphene on SiO_2, which leads to a temperature of 400 K. Hence, there will for such samples be no temperature dependency at temperatures below 400 K [42].

A direct comparison of graphene on hBN versus graphene on SiO_2 is reported in [24], here field-effect mobilities of 140,000 cm^2/Vs have been measured at a low charge carrier density. Furthermore, a temperature dependency was observed at the minimum conductance for temperatures above 15 K given an upper bound of $\tilde{n} \approx 10^9\ \mathrm{cm}^{-2}$ for the residual density. This dependency down to low temperatures indicates that the electron-hole puddles are greatly diminished for hBN supported graphene. Finally, field-effect mobilities up to 140,000 cm^2/Vs have been demonstrated at room temperature in a heterostructure of hBN/graphene/hBN [21]. Here the graphene is both supported by the hBN and also shielded from the environment by the hBN. All in all hBN is an ideal substrate for graphene and also other 2D electronic devices.

2.3 Contacts to 2D Materials

When contacting a 3D crystal with a metal, covalent bonds are normally formed between the contact metal and dangling bonds of the bulk crystal. However, there are no out-of-plane

dangling bonds in pristine 2D crystals, which may lead to large contact resistance [53], and is in general making contacts to 2D crystals more challenging. The principle of ohmic and Schottky contacts is in the following introduced, and the contacts to 2D crystals will be discussed.

Ohmic and Schottky Contacts

With ohmic contact, the current flow follows Ohm's law

$$\mathbf{J} = \sigma \mathbf{E} \ . \tag{2.10}$$

Here, $\mathbf{J}$ is the current density, σ is the conductivity and $\mathbf{E}$ is the electrical field. Ohm's law may also be written as in Eq. (2.4), $V = RI$, where V is the voltage, I is the current and R is the resistance. The I-V characteristic over an ohmic contact is therefore a straight line going through zero, and the resistance is the inverse of the slope.

A Schottky contact is a metal-semiconductor junction where the work function of the metal, ϕ_M, is higher than the elector affinity of the semiconductor, χ, leading to a barrier $\phi_B = \phi_M - \chi$, the Schottky barrier. The I-V characteristics of a Schottky diode in 3D and 2D systems can be described by the current density [54]

$$J = A^* T^\alpha \exp\left(\frac{-e\phi_B}{k_B T}\right)\left[\frac{eV}{\eta k_B T} - 1\right] \ , \tag{2.11}$$

where A^* is Richardson's constant for either 2D of 3D, T is the temperature, α is a geometric factor, 2 for a bulk 3D system and 3/2 for a 2D system. Finally, η is the ideality factor, which for an ideal Schottky diode is unity.

Contacts of metal on the surface of the crystal and contacts only touching the edge of the crystal are distinguished as top contacts and side/edge contacts. Edge contacts have both been modelled [55] and demonstrated experimentally [21] to have the lowest contact resistance, down to 150 Ωμm at high gating.

When electrically contacting TMDs various approaches can been taken. Matching of the metal work function to either the valence or conduction band lowers the Schottky barrier. Hence, a low work function metal is suitable for n-type contacts and high work function metals is suitable for p-type contacts. Utilisation of metals with different work function have shown to enhanced ambipolar behaviour in devices of the TMD WSe_2, where a source electrode of Ni is used to create a n-type contact and a drain electrode of Pd yields a p-type contact [56]. Low contact resistance of 200 Ωμm-300 Ωμm has been reported for MoS_2 by phase engineering. This low contact resistance is obtained by changing the MoS_2 from its semiconducting 2H phase to its metallic 1T phase under the contacts [57].

Since the TMDs are air sensitive encapsulation in hBN is highly favourable for device performance and long-term performance. Unfortunately the 1D edge contacts [21] used for hBN-encapsulated graphene do not work on TMDs, but graphene may be used as an intermediate contact to hBN-encapsulated TMDs [23].

It is an advantage to use graphene as a contact to hBN-encapsulated TMDs, as the work function of graphene is tunable. The work function of monolayer graphene has a square root dependency on the charge carrier density [58]

$$e\phi_{WF}^{Mono}(n) = e\phi_0^{Mono} - \mathrm{sgn}[n]\hbar v_F \sqrt{\pi |n|} \ , \tag{2.12}$$

while multilayer graphene had a linear dependency

$$e\phi_{WF}^{Multi}(n) = e\phi_0^{Multi} - \frac{\pi \hbar^2 n}{2m^*} \ . \tag{2.13}$$

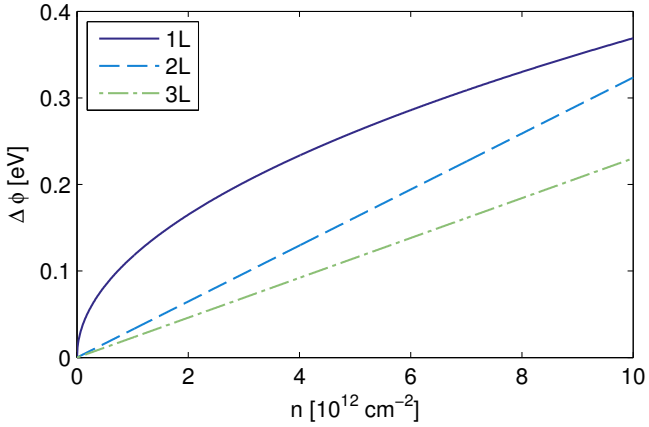


Figure 2.3: *Change in the work function of mono-, bi- and trilayer graphene as a function of gate induced carrier density. The change in work function is the last term of the RHS of Eq. (2.12) for monolayer and Eq. (2.13) for bi- and trilayer. An effective masses of* $m^*_{2L} = 0.037\, m_e$ *and* $m^*_{3L} = 0.052\, m_e$ *have been used for the plots [42].*

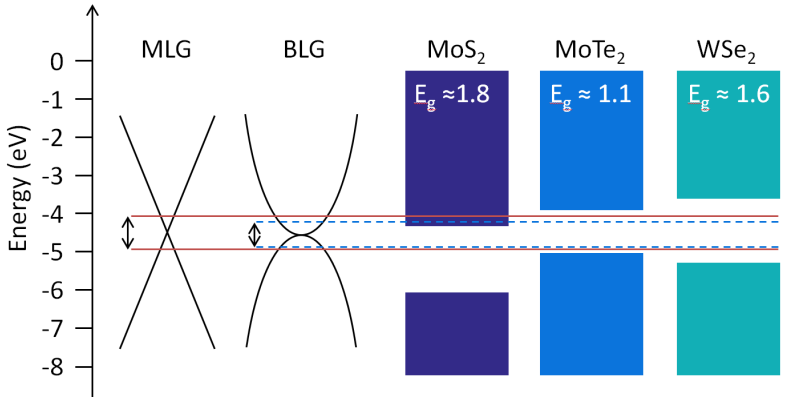


Figure 2.4: *Illustration of the arrangement of the dispersion relation for monolayer (MLG) and bilayer (BLG) graphene and band alignment of monolayer* MoS_2*,* $MoTe_2$ *and* WSe_2*. The tunability of the monolayer and bilayer graphene work function are indicated with the solid and the dashed lines, corresponding to a induced charge carrier density of* $\pm\, 10^{13}\, cm^{-2}$*.*

Here, $\hbar$ is Planck's constant, v_F is the Fermi velocity and m^* is the effective mass of the charge carriers. sgn$[n]$ is -1 for negative gate voltages and $+1$ for positive gate voltages. ϕ_0^{Mono} and ϕ_0^{Multi} are the work function of non-doped mono- and multilayer graphene. This work function is for mono- and bilayer graphene $\phi_0^{MLG} \approx 4.5\,\text{eV}$ and $\phi_0^{BLG} \approx 4.6\,\text{eV}$, respectively [59, 60]. For a doping range of $n = \pm 10^{13}\,\text{cm}^{-2}$, which is easily achieved with a SiO_2 or hBN dielectric, the work function for monolayer graphene can be tuned by $\phi_0^{Mono} \pm 0.37\,\text{eV}$. The work function of bi- and trilayer is less tunable especially for low charge carrier densities due to the linear dependency, see Fig. 2.3.

Monolayer MoS_2, $MoTe_2$ and WSe_2 all have direct band gaps, whereas the bilayer and multilayer flaked have indirect gaps that decrease with number of layers. For instance, monolayer MoS_2 has a gap of $\sim 1.8\,\text{eV}$, whereas the bulk crystal has a gap of $1.2\,\text{eV}$. For $MoTe_2$ and WSe_2 the monolayer gaps are $\sim 1.1\,\text{eV}$ and $\sim 1.6\,\text{eV}$, and the gaps of the bulk crystals are $1.0\,\text{eV}$ and $1.2\,\text{eV}$, respectively [61, 62]. The band gap sizes and positions of the valence band maxima and the conductance band minima depend on the calculation of band structures [17, 18, 63, 64], the general arrangement of the bands are as illustrated in Fig. 2.4. The illustration shows the

band alignment of the three semiconducting TMDs along with mono- and bilayer graphene. The tunability of mono- and bilayer graphene is illustrated with solid and the dashed lines, respectively. It is clear from the illustration that electron transport should be achievable for MoS_2 with graphene contacts, whereas hole transport should not be obtainable with graphene contacts. The range of the tunable work functions for mono- and bilayer graphene is approximately in the middle of the band gap of $MoTe_2$ and WSe_2 and ambipolar transport is therefore possible. This is a simple picture and the range of the work functions also depends on initial doping of the graphene, position of the gate and potential screening by metal leads and other flakes in the vdW heterostructure.

2.4 Transport Measurement

Electrical characterisation of 2D crystals have been done both with two-terminal and four-terminal field-effect measurements. A great advantage of the four-terminal measurements is that the contact resistance can be excluded. This section introduces the principles of two-terminal and four-terminal measurements.

2.4.1 Two-Terminal Measurements

The total resistance, R_{tot}, measured over a device with a two-terminal measurement, can be expressed as

$$\begin{aligned} R_{tot} &= \frac{V}{I} \\ &= 2R_C + R_{ch} \\ &= 2R_C + \frac{L/w}{ne\mu} \ , \end{aligned} \tag{2.14}$$

where, V are the voltage drop across the device and I is the current measured in the device, R_{ch} is the resistance of the device channel, and the resistance of the two contacts, R_C, are assumed equal. L and w is the length and width of the device channel, e is the elementary charge and n is the carrier density induced by the gate.

The approach of [46, 65] have been employed to avoid underestimating the field-effect mobility, μ. This approach assumes a gate independent contact resistance, which is generally not the case as the contact resistance generally is higher close to the Dirac point of graphene [66, 67]. While the field-effect mobility is still underestimated the error is reduced by this approach. The hole and electron branches of the conductance versus gate voltage measurement are fitted independently to find both the hole and electron carrier mobility. An example of raw data and fits are seen in Fig. 2.5 together with device schematic. For details of the fitting see supplementary text of [46].

2.4.2 Four-Terminal Measurements

The channel resistance and contacts resistance can be distinguished from each other in four-terminal measurements. Device geometries like the one shown in Fig. 2.6a-b are often used for four-terminal measurements. A constant voltage drop is applied between the source and drain electrodes, marked S and D in Fig. 2.6a, while measuring the current through the device as well as the voltage drop between to voltage probes, marked V_{xx} in Fig. 2.6a. Alternately a constant current may be applied between the source and drain electrodes, while measuring the voltage drop over both the source and drain and the four-terminal voltage probes.

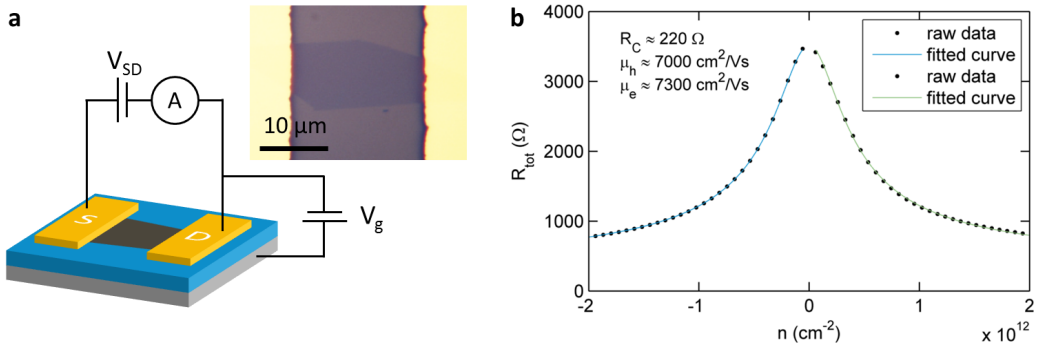


Figure 2.5: *(**a**) Schematic of two-terminal device and measurements configuration together with optical micrograph of a two-terminal graphene stencil device on a substrate of highly doped silicon with a layer of 300 nm SiO_2. (**b**) Raw data from graphene device and fitted lines to obtain an estimate of R_C, μ_h and μ_e. The hole and electron branches are fitted individually.*

The resistivity of the device channel, ρ, is found from the voltage measured at the voltage probes, V_{xx}, and the current flowing through the device, I_{SD},

$$\begin{aligned}\rho &= R_{xx}\frac{w}{L_{vp}} \ , \\ &= \frac{V_{xx}}{I_{SD}}\frac{w}{L_{vp}} \ ,\end{aligned}$$

where R_{xx} is resistance measured at the four-terminal voltage probes, w is the width of the channel and L_{vp} denotes the channel length between the probes. The mobility can then be found by applying this to Eq. (2.7), $\sigma = ne\mu$ as $\rho = 1/\sigma$ and $n = V_g C/e$, Eq. (2.3). The field-effect mobility estimated from the slope of the conductance versus applied gate voltage is then

$$\begin{aligned}\mu(n) &= \frac{\sigma(n)}{ne} \ , \\ \mu(V_g) &= \frac{\delta G_{xx}}{\delta V_g}\frac{1}{C}\frac{L}{w} \ .\end{aligned}$$

The mobility is in practice calculated as a function of V_g by fitting a straight line to an interval of the conductance around the V_g. The voltage terminals on either side of the channel, V_{xy}, is used for magneto-transport measurements, where a magnetic field is applied perpendicular to the sample surface.

The average contact resistance for a device with a constant width, w, can be estimated by subtracting the resistance of the full channel from the two-terminal resistance measured at the source-drain electrodes, R_{SD},

$$R_C = \frac{1}{2}\left(R_{SD} - \rho\frac{L_{SD}}{w}\right) \ , \tag{2.15}$$

$$= \frac{1}{2}\left(R_{SD} - R_{xx}\frac{L_{SD}}{L_{vp}}\right) \ , \tag{2.16}$$

where L_{SD} is the channel length between the source-drain electrodes.

The contact resistance may also be found via transfer length measurement (TLM). Here, a series of two-terminal measurements on devices channels of various lengths are performed. Both the contact resistance and the sheet resistivity can be estimated with the TLM technique, see graph in Fig. 2.6c.

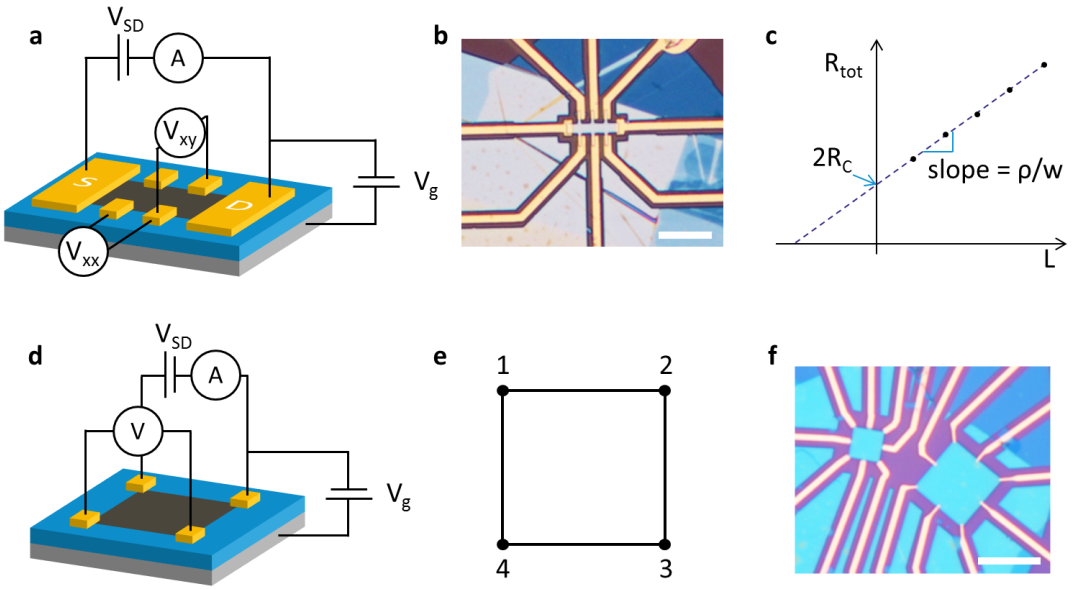


Figure 2.6: *Device geometries and electrical setups for four-terminal measurements. The number of charge carriers in the device channel is controlled by a metallic gate separated from the channel by a gate dielectric. (**a**) A voltage drop is applied between the source and drain electrodes while measuring the current, and the voltage drops V_{xx} and V_{xy}. (**b**) Optical micrograph of a device of hBN-encapsulated graphene on which four-terminal electrical measurements are performed. (**c**) Illustration of the result of a transfer length measurement, the contact resistance and the resistivity of the channel are found from the intersect and the slope of the measurements, respectively. (**d**) Outline of the vdP measurement method on a devices of square geometry with small contacts in the corners, the contacts are numbered as in (**e**). (**f**) Optical micrograph of two square devices of hBN-encapsulated graphene contacted with 1D edge contacts. The scale bars of (**b**) and (**f**) are 10 μm.*

The van der Pauw Method

The conductivity of arbitrary shaped samples can be determined with the van der Pauw (vdP) method provided the following conditions are met [68].

1. Contacts shall be placed at the circumference of the sample
2. The contacts shall be small relative to the side length of the device
3. The sample shall be homogeneous in thickness
4. The sample shall be continuously

Point 1 and point 2 may be fulfilled by appropriate design of the metal electrodes made on the device, and point 3 is indeed satisfied in 2D flakes. Point 4, on the other hand, is assumed satisfied, especially on flakes exfoliated from bulk crystals, as these are assumed to have few defects. However, there may be creaks, uni-axial strain, local doping, etc. leading to a non-continuous sample. Devices of square geometries with the contacts located in the corners as illustrated in Fig. 2.6d-f, are often used for the vdP method.

The resistance $R_{ab,cd}$ is defined as the resistance measured when a current is send from contact a to contact b, and the voltage drop is measured from contact c to contact d. Ohm's law gives the resistance

$$R_{ab,cd} = \frac{V_{cd}}{I_{ab}} \ .$$

The sheet resistivity, ρ_S (units of Ohms per square, $\Omega/\square$), is found with the vdP formula by measuring the resistance in two configurations $R_{12,34}$ and $R_{23,41}$.

$$e^{(-\pi R_{12,34}/\rho_S)} + e^{(-\pi R_{23,41}/\rho_S)} = 1 \ . \tag{2.17}$$

The contacts are numbered as in Fig. 2.6e. On a symmetric device $R_{ab,cd} = R_{cd,ab}$, known as the reciprocal theorem. The horizontal and vertical resistance is gained by measuring in the two reciprocal configurations and averaging

$$R_h = \frac{R_{12,34} + R_{34,12}}{2} \ ,$$
$$R_v = \frac{R_{23,41} + R_{41,23}}{2} \ .$$

The sheet resistivity is found as in Eq. (2.17)

$$e^{(-\pi R_h/\rho_S)} + e^{(-\pi R_v/\rho_S)} = 1 \ . \tag{2.18}$$

Finally, the sheet resistivity can be approximated as $\rho_S = \pi R_{h,v}/\ln(2) \approx 4.52 R_{h,v}$, in the case where R_h and R_v are the same.

2.5 Electrical Measurement Setups

Three experimental setups have been used for I-V, two- and four-terminal field-effect measurements. All three setups are equipped with coaxial cable to reduce electrical noise. A probe station, located at DTU Danchip, was used for measurements under ambient conditions. In this setup, tungsten probes are aligned with micro-manipulators to the contact pads of the sample, up to eight probes are available at the set-up. Furthermore, an electrical set-up build around a customised Linkam LTS600P controlled atmosphere stage equipped with electrical feedthroughs and a built-in cooling/heating element is used. The sample stage temperature is cooled with liquid nitrogen. The temperature can be varied from 77 K to 873 K (600 °C). The closed chamber allows the ambient air to be replaced by a dry pure neutral gas, such as nitrogen, and a vacuum down to ~ 0.3 bar can be applied. Finally, a TeslatronPT from Oxford instruments is used for low temperature and magneto-transport measurements. In this setup temperatures from 300 K down to 1.5 K and magnetic fields up to 12 T are achievable. In all setups, Keithley sours meters are used for applying the gate and source-drain voltage, and Keithley multimeter is used for measuring the voltage drop in four-terminal measurements.

3 Characterisation

The 2D flakes are randomly distributed on the substrate after mechanical exfoliation. Optical microscopy is therefore a powerful tool for fast and non-destructive localisation and inspection of the thin flakes. Raman spectroscopy, atomic force microscopy, scanning and transmission electron microscopy provides more detailed information on the condition and quality of the flakes, but in much smaller areas compared to the optical microscopy. This chapter covers the basic concepts of these five characterisation tools.

Contents

3.1 Optical Microscopy

A monolayer graphene flake absorbs 2.3 % of the incoming light [69], hence it is almost transparent. Fortunately, the contrasts of the thin flakes are enhanced when the flakes are supported by a suitable substrate, making it relatively easy to locate the down to one atom thin flakes. The contrast $C(\lambda)$ of a 2D flake on a substrate is found from

$$C(\lambda) = \frac{I_s(\lambda) - I(\lambda)}{I_s(\lambda)} \ , \tag{3.1}$$

where $I_s(\lambda)$ is the intensity of the light reflected from the substrate, and $I(\lambda)$ is the intensity of the light reflected from the 2D flake. The intensity of the reflected light depends on the refractive index and thickness of the materials in the sample, as well as the wavelength λ of the microscope light [70]. The wavelength-dependent contrast of monolayer graphene on a silicon substrate with 0 nm to 350 nm of SiO_2 is plotted in Fig. 3.1. It is apparent from the surface plot that a substrates of silicon with either ~ 90 nm or ~ 300 nm SiO_2 are suitable for

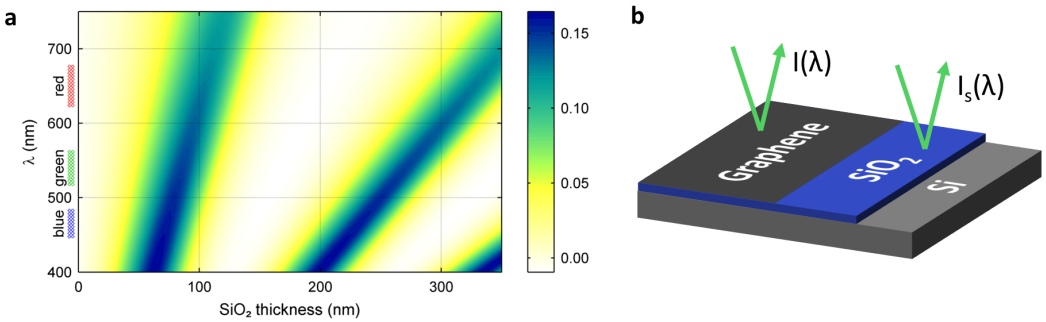


Figure 3.1: (**a**) *Surface plot of the contrast of monolayer graphene dependence on the* SiO_2 *thickness and the wavelength of the incident microscope light, from [70].* (**b**) *Sketch of the geometry.*

exfoliation of graphene, as the contrast for these SiO_2 thicknesses is enhanced for a wide range of wavelengths.

In a microscope image, the pixels captured are constructed from a red, green and blue component. The wave dependent contrast from Fig. 3.1 can be converted into a pixel contrast by taking the spectral response function of the microscope camera into consideration. For instance, monolayer graphene on 90 nm SiO_2 have a contrast of 9 %, 10 % and 8 % for the red, green and blue pixel, respectively. The same SiO_2 thicknesses are applicable for monolayer TMDs. The contrast of various TMDs will differ due to the difference in refractive index and thickness.

Recording of optical images under dark field illumination is an important tool for inspection of the conditions of the flakes. Dark field images are constructed from the light scattered by the sample, hence edges and particles will scatter more than flat surfaces and be brighter. Edges of monolayer crystals on SiO_2, cracks within the flake, tape residues and particles on the flake are detectable with dark field illumination. Optical images are here mainly captured with a Nikon ECLIPSE L200N optical microscope.

3.2 Raman Spectroscopy

The basic concept of Raman spectroscopy of graphene is presented here. For more details, the review by A. C. Ferrari and D. M. Basko [71] is recommended. Raman spectroscopy is a widespread characterisation method within the graphene research community.

In Raman spectroscopy, the sample is illuminated with a laser beam. The photons of the laser light interact with vibrational modes (phonons and other excitations) in the sample via inelastic scattering, resulting in a measurable energy shift of the photons collected after the interaction with the sample. The vast majority of photons which undergo elastic scattering (Rayleigh scattering) which is filtered out from the collected light.

The Raman spectrum contains various peaks, which are characterised by the peak position (Pos), full width at half maximum (FWHM), and peak intensity (I) with respect to other peaks. Raman spectra of pristine and defected graphene are seen in Fig. 3.2a. The G peak at $\sim 1580\,\mathrm{cm}^{-1}$ correspond to an in-plane optical mode at the Γ point, see illustration in Fig. 3.2b. The D peak ($\sim 1350\,\mathrm{cm}^{-1}$) originate from inter-valley scattering (between K and K'), which requires a defect for its activation. The D mode corresponds to the breathing mode of the six-atom carbon ring see Fig. 3.2c. The mode of intra-valley scattering is named D', and appear close to the G peak at $\sim 1620\,\mathrm{cm}^{-1}$. The 2D (2D') is overtone of the D (D') peak, and is at a Raman shift of $\sim 2700\,\mathrm{cm}^{-1}$ ($\sim 3250\,\mathrm{cm}^{-1}$). The 2D and 2D' do not require a defect to be activated as they originates from momentum-conservation of a two-phonon process [71].

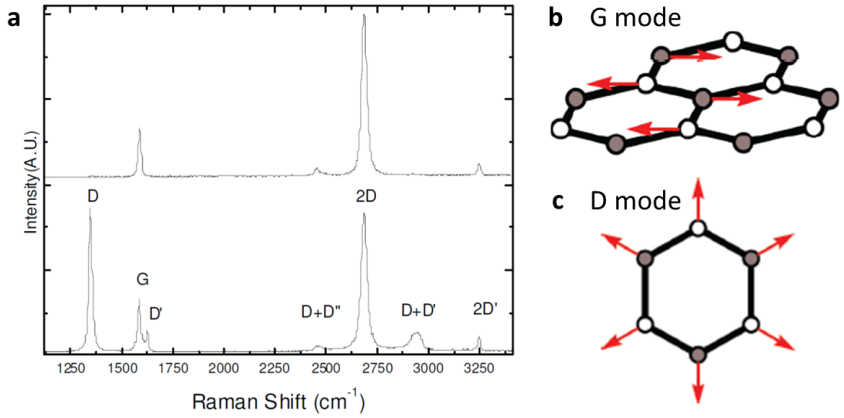


Figure 3.2: *(**a**) Raman spectrum of pristine (top) and defected (bottom) graphene. Illustration of the atom displacement (indicated with red arrows) for the (**b**) G and (**c**) D mode. Adapted from [71].*

The occasionally used peaks D+D' ($\sim 2950\,\mathrm{cm}^{-1}$) and D+D" ($\sim 2450\,\mathrm{cm}^{-1}$) are the peaks assigned to the combination of D with D' or D". The D" is a longitudinal acoustic phonon appearing at $\sim 1100\,\mathrm{cm}^{-1}$.

When collecting Raman spectra of hBN-encapsulated graphene or graphene on hBN one should be aware that the Raman signal of hBN has a peak at $\sim 1370\,\mathrm{cm}^{-1}$ hence close to the D peak of graphene [72]. In pristine graphene the G and 2D peaks will be dominating, and the peaks of the 2D' and D+D" mode will also be present. In defected graphene the peaks requiring a defect to activate will appear, hence D, D' and D+D'. The most often used peaks to analyse graphene Raman spectra are the G, D and 2D peak.

The intensity ratio I(D)/I(G) is a measure of how defected the graphene is. I(D) increases as graphene becomes more defected, however only to a certain degree as the intensity of the D-peak will start to decrease when the graphene becomes so disordered that the rings of six carbon atoms start to break up. I(G) is more or less constant as it relates to the motion of sp^2 carbons. The FWHM of the G peak increases with disorder, and can therefore in combination with the I(D)/I(G) ratio be used to discriminate between lightly and highly disordered samples. The FWHM of 2D peak is also of interest, as a low FWHM(2D) indicate areas of potentially high carrier mobilities in stacks of hBN-encapsulated graphene [73].

A DXR Raman Microscope from Thermo Scientific with a 455 nm excitation laser is used for the Raman characterisation in this report. A power of 1 mW and multiple exposures of 20 s to 30 s are typically used. Raman spectroscopy has been used for inspection of flakes both on SiO_2 and after encapsulation in hBN, and for characterisation of fluorinated graphene, see Sec. 5.1.3.

3.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is in particular due to its sub nanometer height resolution useful in the research field of 2D materials. In AFM a cantilever with a sharp tip is moved over the sample, and the position of the cantilever is controlled with piezoelectric elements. A laser beam is aligned to the cantilever and reflected on to a photodiode to probe changes in the deflection of the cantilever.

The most common AFM modes are contact and tapping. In contact mode, the tip is moved (dragged) over the sample. The cantilever can either be held at a fixed position measuring the height by the deflection of the cantilever, or moved in the z-direction according to the

topography of the sample through, a feedback loop adjusting the height. Contact mode can be destructive to the sample and AFM tip, and can also drag polymers or other residues across the surface not yielding the actual typography. The gentler tapping mode is therefore often preferred, and the main mode used for AFM inspections here.

In tapping mode AFM, the cantilever is alternated at (or close to) its resonant frequency, and brought close to the surface of the sample. The amplitude of the cantilever vibration is affected by the nearby surface. Generally the amplitude decreases when the surface gets closer and increases when the distance to the surface increases. A feedback loop adjusts the height to insure constant amplitude, and the topography map of the sample is constructed from the amplitude variations. The amplitude may also be affected by chemical differences in the sample resulting in an apparent typography different from the actual typography.

Beside the surface topography the phase shift between the signal driving the cantilever and the output signal can be used to map surface properties. The phase shift often shows a strong contrast of material properties such as elasticity, adhesion and friction, and can therefore be used to construct chemical map based on the material differences [137]. Topographical differences may also appear in the phase contrast AFM as the adhesion will increase at steps as a larger area of the tip is close to the sample surface.

Topography AFM inspections have been used to measure the thickness of various flakes, in particular hBN flakes, as the thickness of the hBN flakes are important for field-effect gating and nano-patterning of devices. Mainly hBN flakes of 5 nm to 30 nm are of interest for devices. Thin flakes of graphene and TMDs are normally not inspected by AFM to find their thickness but to examine the condition of the flakes with respect to contamination, corrugations to the substrate and degradation. Specifically, the height measured from thin flakes to the substrate may be miss guiding due to chemical contrast and water trapped between the flake and the substrate. Trapped water under the flakes will make the flakes appear thicker. Chemical contrasts between the substrate and the flake may also lead to an apparent thickness larger than the expected thickness [1, 74]. The number of layers in mono- to few-layer graphene and TMD flakes is therefore mainly assessed by their contrast in optical microscopy. Furthermore, phase contrast AFM have in this thesis been found applicable for detection of exposed versus covered edges in multilayer TMD flakes, this result is presented in Sec. 6.1.

AFM scans have been performed both in a Dimension Icon-PT from Bruker AXS and a NTEGRA scanning probe microscope from NT-MDT with a Smena measuring head. Scans are mainly performed in tapping mode with typical parameters of a driven frequency of 235 kHz, a magnitude of 10 nA, a set point of 5 nA and scan speed of $10 - 30\ \mu$/s.

3.4 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is a microscopy technique where a focused beam of electrons is scanned across the sample surface constructing an image. The electrons of the focused beam (primary electrons) interact with the sample specimen in a teardrop-shaped interaction volume. The size of the interaction volume will depend both of the energy of the primary electrons and the atomic number of the specimen. An increase in energy will increase the size of the volume and an increase in atomic number will decrease the volume. One pixel is created by the detection of electrons being emitted from the interaction volume.

Detection of reflected primary electrons, also called backscattered electrons, is used to image variations in the composition of the sample. This detection is possible as heavy elements will backscatter more primary electrons compared to lighter elements. The backscatter electron detector is located above the sample in order to collect the high energy electrons.

Interaction of the primary beam with the specimen leads to ejection of low energy electrons from the atom in the specimen, called secondary electrons. Secondary electrons close to the

surface can escape the sample. Edges and slopes will appear brighter as a larger part of the interaction volume is close to the surface and more electrons can therefore escape. Information about the surface topography is therefore gained by detection of secondary electrons. A secondary electron detector is located to the side in the SEM chamber, and the low energy secondary electrons are directed towards the detector by a large voltage bias. Furthermore, a secondary electron detector is located inside the lens, named the Inlens detector, a short working distance is needed when using the Inlens detector. Mainly the Inlens detector has been used with a short working distance of ~ 2 mm to maximise the number of electrons entering the detector and thereby obtain high resolution images.

SEM is a very powerful tool for sample characterisation, however there are some drawbacks. Most 2D samples are located on the electrically insulating SiO_2, which may lead to accumulation of electrostatic charges, leading to drift and lower resolution. Samples can be sputter-coated with a thin layer of conductive material; however this is seldom favourable as it may destroy the sample. Furthermore, amorphous carbon gets deposited on the sample surface when imaging. SEM inspections have therefore only been performed on devices after electrical characterisation, not to influence the performance of the device. SEM inspections have also been used in a great extent for optimisation of nano-structuring in both silicon and hBN. Nano-structures of periodic lattices of holes with periods of sub 30 nm have been characterise, see results in Sec. 5.3.1. Microscopes at the DTU Danchip cleanroom facility have been used.

3.5 Transmission Electron Microscopy

Variation in transparency to electrons can be imaged with transmission electron microscopy (TEM). Thin samples are required as electrons are transmitted through the sample. Heavy elements will appear dark compared to lighter elements as more electrons will scatter on the heavier elements. Light elements such as carbon can be difficult to image as they have a smaller contrast and a higher dose is therefore needed to obtain a sufficient signal-to-noise ratio. However, the high energy electron irradiation can create knock-on damage to the crystal, and at a higher dose (current per area) will consequently lead to more damage. For defect-free graphene, acceleration voltages below 80 keV is below the threshold for knock-on damage for sp^2 carbon [75]. Atomic resolution is obtainable in TEM providing information about crystallographic orientation, and imaging vacancies as well as other defects.

Cross-section of thin samples can also be imaged, which requires a section of a sample to be cut out by focus ion beam milling in a SEM and placed on a TEM grid. This technique has here used to inspect the interfaces in-between layers of a van der Waals stacked heterostructure. Specifically, the detection of exposed versus covered edges detected by phase contrast AFM have been confirmed by cross-sectional TEM, see Sec. 6.1. A Tecnai T20 G^2 microscope operated at 200 kV have been used in this work, the microscope is located at the DTU center for electron nanoscopy (DTU Cen).

4 Fabrication

Monolayer crystals are produced by mechanical exfoliation from bulk crystals and stacked by the interlayer van der Waals forces to create heterostructure. These structures are further processed to create electrical contact to the crystals. This chapter gives a detailed description of the techniques used to exfoliate flakes and assemble vdW heterostructures, and of the fabrication steps involved in contacting these flakes and stacks electrically.

Contents

4.1 Exfoliation of 2D Crystals

Flakes of graphene, hBN and various TMDs are mechanically exfoliated from bulk with the scotch tape method [2, 70]. Bulk crystals of graphite and the three TMDs; MoS_2, $MoTe_2$ and WSe_2 are seen in Fig. 4.1. Exfoliation may be done with various tape types, mainly two types of tape are used here; 3M Scotch ® 810 Magic^{TM} Tape (referred to as scotch tape) and blue

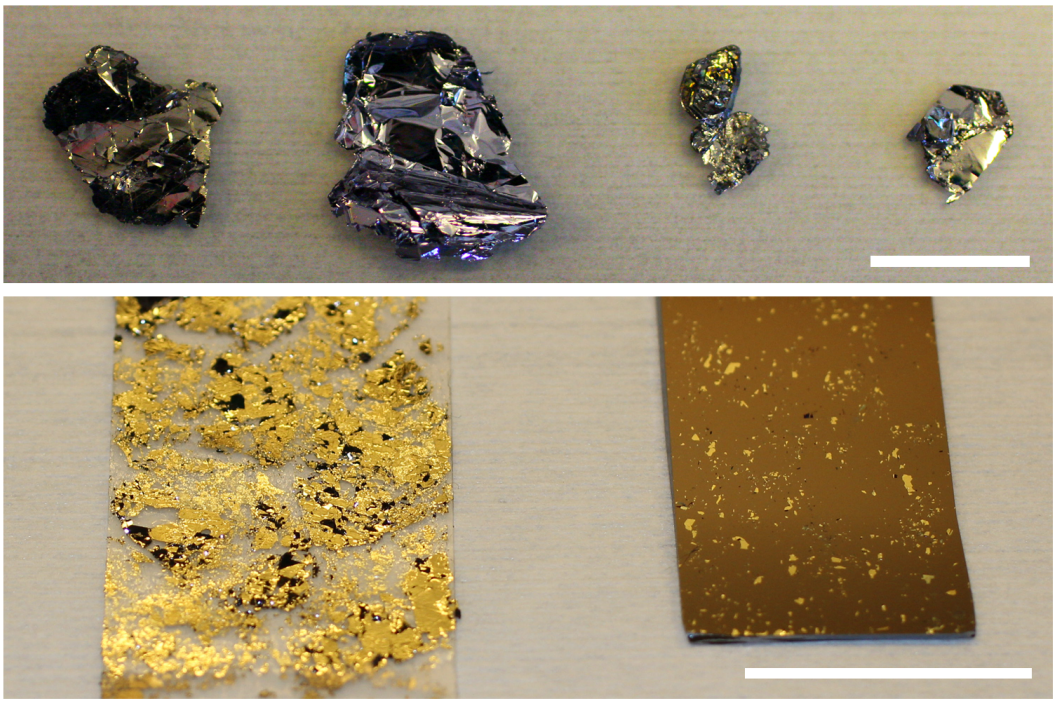


Figure 4.1: *(Top) Bulk crystals of graphite, MoS_2, $MoTe_2$ and WSe_2, from left to right. (Bottom) Graphite distributed on scotch tape and Si/SiO_2 chip after exfoliation with the tape. The scale bars are 1 cm.*

semiconductor wafer tape SWT20+ from Nitto Denko (referred to as blue tape). To prepare tape for exfoliation, a bulk crystal is repeatedly adhered to the tape and removed again with tweezers, and thin parts of the bulk crystal will in this fashion be distributed on the tape. A second piece of tape is applied on top of the tape to make a "copy" which will be applied to a cleaned silicon dioxide, SiO_2, substrate, see tape for exfoliation and chip after exfoliation in Fig. 4.1. Several copies can be made before the tape has to be discarded.

The SiO_2 substrate is cleaned prior to the exfoliation to increase the yield and size of flakes and to minimise the amount of trapped water and hydrocarbon species between the flakes and the substrate [76]. Cleaning involves a bake at 200 °C to evaporate water from the surface followed by an oxygen plasma. Two plasma asher systems are used; PlasmaEtch PE-50, 5 minutes, pressure of 300 mbar O_2 and power of 120 W, and a TePla Plasma Asher model 300 (at DTU Danchip), 10 minutes, gas flow 200/50 sccm O_2/N_2 and a power of 400 W. The tape is immediately applied to the SiO_2 surface after the plasma treatment. The tape may be rubbed to increase the yield; however, this should be done gently to avoid fractured flakes. To release the tape from the SiO_2 surface, the scotch tape is peeled of slowly at a low angle, and the blue tape is peeled off in the same manner while heated to 85 °C on a hot plate, as heating lowers the adhesion of the blue tape.

Exfoliation with scotch tape generally yields more and larger flakes, but it also leaves a large amount of tape residues on the SiO_2 surface. The blue tape gives a smaller yield, but a cleaner SiO_2 surface. The selection of tape will therefore depend on the application of the produced flakes [20]. Examples of exfoliated graphene, hBN and WSe_2 flakes are shown in Fig. 4.2. Mono- and bilayer graphene are easily distinguishable, whereas sub 2 nm hBN is difficult to see on $\sim$ 90 nm SiO_2 due to a far smaller absorption. A collection of optical micrographs shown in Fig. 4.2d illustrates the change in colour of hBN as the thickness increases. The contrast of WSe_2, and TMDs in general, changes significantly with the number of layers, visualised by segments of microscope micrographs in Fig. 4.2e.

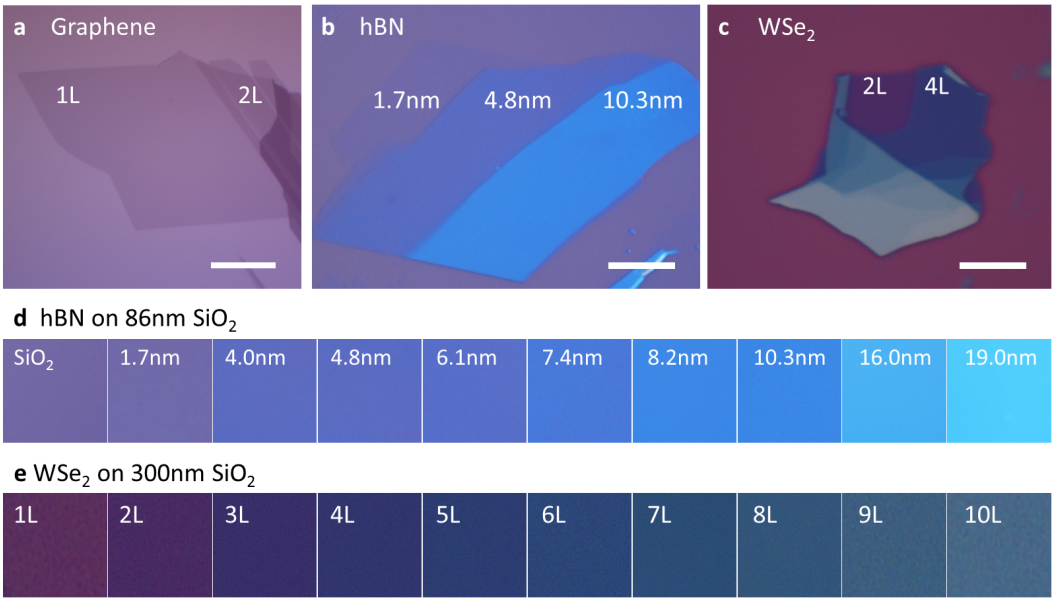


Figure 4.2: *Examples of exfoliated 2D flakes of (**a**) mono- and bilayer graphene, (**b**) hBN flake with three regions of different thicknesses and (**c**) a WSe_2 flake. (**d**) Colour scale of hBN flakes of versus thickness on 86 nm SiO_2, the flake thicknesses are measured by AFM. Scale bars are 10 μm. (**e**) Layer dependent contrast for one to ten layers of WSe_2 flakes on 300 nm SiO_2. The colour scales in (**d**) and (**e**) are made from segments of optical micrographs of flakes.*

4.2 van der Waals Heterostructure Assembly

Assembly of mono- and multilayer flakes makes it possible to controllably create heterostructures with atomic layer precision. Interlayer van der Waals (vdW) forces are employed to lift one flake up with another flake. This assembly method produces atomically clean interfaces between stacked flakes, which results in excellent device performance [20, 21, 23, 73, 77]. The vdW forces and how the assembly work is discussed further in Sec. 4.2.6.

Flakes are lifted (pick-up) and released (drop-down) with a polypropylene carbonate (PPC) coated polydimethylsiloxane (PDMS) block in order to construct the heterostructures. A micromanipulator which is mounted on a microscope stage, see Fig. 4.3a, is used to control the movement of a glass microscope slide on which the PDMS/PPC block is mounted. The micromanipulator can move the slide in the x, y and z direction and tilt the slide allowing for alignment to the flakes and approach at various angles.

Stacks are built from the top and down, meaning the first flake to be picked-up, will be the top-hBN layer of the final stack. The top-hBN flake is then used to pick-up the next flake by first dropping down the top-hBN on the flake and then picking up both flakes, by means of van der Waals forces between the flakes. The flake(s) composing the device channel, often graphene or a TMD, will in this way be protected by the top-hBN from getting in contact with the PPC and other polymers and chemicals used during device fabrication.

It is not feasible to pick up monolayer flakes with the PDMS/PPC block, both because the monolayer flakes tend to adhere too strongly to the SiO_2 surface, but also because the monolayer flakes often curl up when on the PPC.

The four main steps of van der Waals heterostructure assembly are the pick-up, de-wrinkle bake, drop-down and adhesive bake. These four steps are repeated for each flake included in a stack. Thus, two repetitions are needed to assemble a hBN/graphene/hBN stack, as illustrated

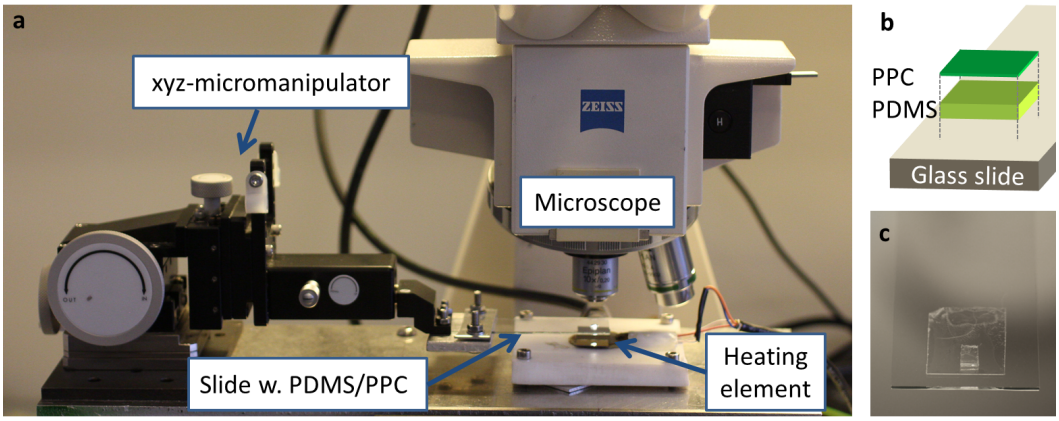


Figure 4.3: *(**a**) Microscope setup with micromanipulator and a combined vacuum chuck and heating element for van der Waals heterostructure assembly. (**b-c**) Illustration and image of glass microscope slide with a block of PPC coated PDMS for pick-up and drop-down of flakes.*

in Fig. 4.4. Preparation of the glass slides used for stacking and the four steps are described in details in the following sections.

4.2.1 Preparation of PDMS/PPC Blocks

The PDMS is prepared from SYLGARD ® 184 by thoroughly mixing ten parts base and one part curing agent. The mixture is applied to a plastic petri dish, $\sim 120\,\mathrm{mg/cm^2}$ to achieve a desired thickness of $\sim 1\,\mathrm{mm}$. The mixture is degassed in a vacuum desiccator for at least two hours, before being cured at 70 °C for 24 hours.

The adhesion between the PDMS and PPC is increased by giving the PDMS a short oxygen plasma prior to spinning the PPC on the PDMS. (PlasmaEtch PE-50, 15-30 seconds, pressure of 300 mbar O_2 and power of 120 W). This reduces the risk of delamination of the PPC during stacking. Double-sided tape or epoxy glue is used to attach a $1\,\mathrm{mm^2}$-$4\,\mathrm{mm^2}$ piece of PPC coated PDMS to a glass microscope slide, see Fig. 4.3b-c.

4.2.2 Step I: Pick-Up

Pick-up is the action of lifting a flake from its exfoliation substrate, illustrated in Fig. 4.4a. The top-hBN, is picked up directly with the PPC. The following flakes are picked up with the top-hBN flake utilising van der Waals forces between the flakes. Only the top-hBN flake will therefore get contaminated with PPC.

PPC is used because it has a low glass transition temperature, $\sim 40\,°\mathrm{C}$, allowing the PPC to re-float when heated. Moreover, PPC will also mould itself to the surface when cooled down after heating as it is a thermoplastic. The moulding of the PPC to the flake(s) increases the adhesion between the PPC and the flake, which need to be larger than the adhesion between the flake and the substrate for the pick-up to be successful. The adhesion forces between the substrate, thin/thick flakes and the PPC are discussed further in Sec. 4.2.6.

When choosing flakes for stacking, the colours of the flakes under bright field illumination are used to estimate the thickness, see Fig. 4.2. Mono- to few-layer graphene and TMD flakes and hBN flakes of $20\,\mathrm{nm} \pm 10\,\mathrm{nm}$ are normally used. The flakes are also inspected with dark field optical microscopy, as contamination such as tape residues and cracks in the flakes are easily spotted and thus the optimal flakes can be chosen. Example of discarded graphene and hBN flakes are seen in Fig. 4.5a-b and Fig. 4.5c-d, respectively. The outline of the graphene

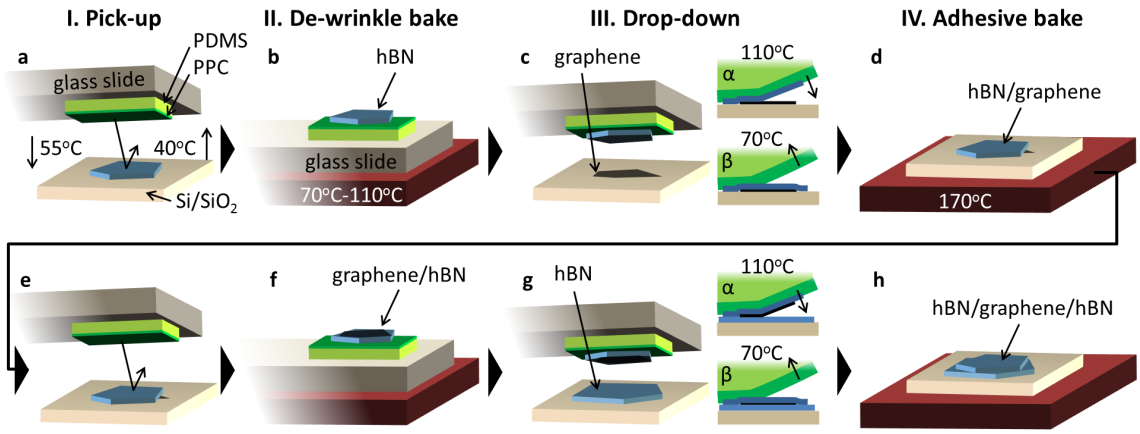


Figure 4.4: *Illustrations of the steps needed to create a hBN/graphene/hBN stack. The four steps of the van der Waals heterostructure assembly is repeated twice for a hBN/graphene/hBN stack. (**a**) The top-hBN is picked-up with the PDMS/PPC block by approaching at 55 °C, cooling down to 40 °C and rapidly moving the glass slide up. The glass slide is flipped around and (**b**) baked to remove wrinkles in the flake before it is (**c**) aligned and dropped-down on the graphene flake. The drop-down is performed by slowly moving the PPC front over the flakes at 110 °C, and then retreating the PPC front at 70 °C leaving the flake behind. (**d**) The hBN/graphene is then baked at 170 °C before the hBN/graphene is picked-up as a single unit (**e**). (**f**) The hBN/graphene is baked on the slide to remove wrinkles before it is (**g**) aligned and dropped down on the bottom-hBN to fully encapsulate the graphene. The finished stack (**h**) is baked, trapped contamination will accumulated in blisters and appear optically after the bake.*

flake is clear in the dark field micrograph, moreover contamination on the SiO_2 as well as lines going through the graphene flake is also apparent, see indications with arrows in Fig. 4.5b. The outline of the hBN is more pronounced in the dark field micrograph as the flake is thicker, see Fig. 4.5d. Furthermore, contamination is easily spotted on the hBN flake, whereas it is difficult to see in the bright field micrograph.

To pick up the top-hBN flake, a Si/SiO_2 chip with exfoliated hBN is fixed on the combined vacuum and heating element under the microscope, and a suitable flake is approached with the PDMS/PPC block on the glass slide. The glass slide is kept parallel to the chip. When approaching, the heater is at room temperature. The micromanipulator is used to bring the PDMS/PPC block in contact with the chip surface. A corner of the PPC will often touch first. The block is lowered further letting the PPC-sample contact area increase and the PPC front proceeds until it is in the proximity the hBN flake. The chip is then heated to 55 °C, and the front will move by itself across the flake. The micromanipulator can be used to lower the glass

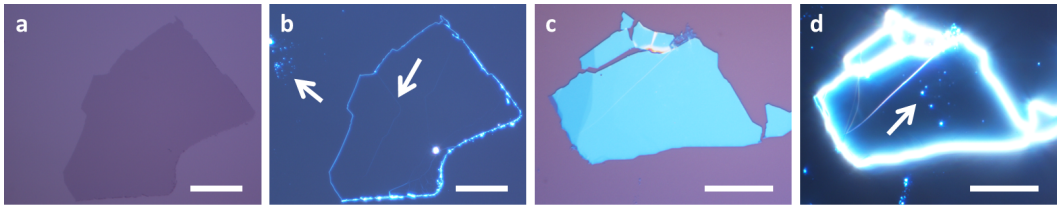


Figure 4.5: *Optically micrographs of monolayer graphene and ∼ 25 nm thick hBN on 86 nm SiO_2. The micrographs of (**a**) and (**c**) are bright and (**b**) and (**d**) are under dark field illumination. Arrows indicate contamination and cracks, scale bars are 20 µm.*

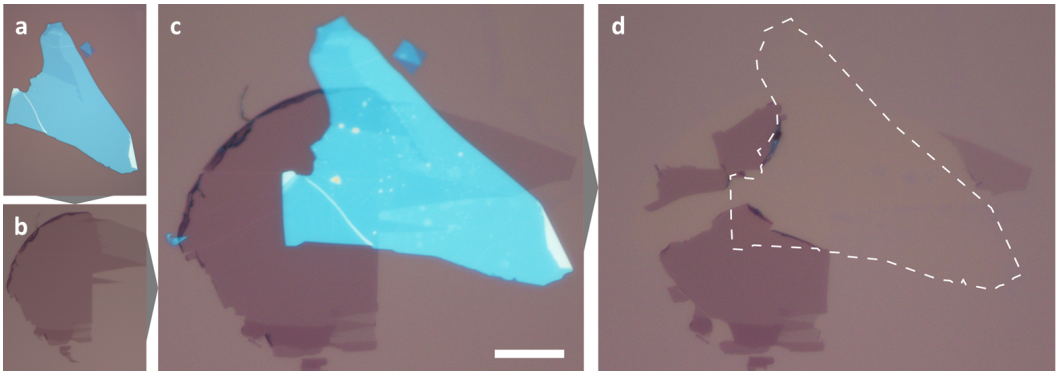


Figure 4.6: *Flakes of (**a**) hBN and (**b**) graphene. (**c**) hBN dropped down on bilayer graphene. (**d**) Substrate after pick-up, the position of the hBN is outlined, only graphene under the hBN is picked-up. Scale bars are 20 µm. Published in [20].*

slide further if the front stops moving. When the front has moved ~ 200 µm past the flake it is stopped by lifting the glass slide slightly up, and the heater is turned off. The sample is cooled down with the PPC in contact to $\sim 40\,^{\circ}\mathrm{C}$, and then the slide is moved up in order to detach the PPC. It is important that the entire PPC contact area releases at once leading to a "snapping" motion. The PPC will adhere too well to the chip if the whole PDMS/PPC block is brought in contact, making it difficult to snap the PPS off the chip surface. A contact area of $\sim 50\,\%$ of the block is suitable.

If the PPC does not snap, but instead the front moves backwards continuously or in small steps, it wills not pick-up the flake. The lack of the snapping motion may be a result of the temperature being too high, the PPC not being parallel to the sample surface or the slide being moved up too slow. The snapping motion may also occur without the flakes being picked up. This is often a result of too high adhesion between the flake and SiO_2 surface. Adhesion of the flake to the substrate can be lowered by immersing the chip immersed in heated acetone for half an hour.

Furthermore, lithographically pre-patterned 2D flakes can also be picked-up [20], see Fig. 4.7. It is a great advantage to be able to pre-pattern flakes prior to encapsulation, as the exfoliated flakes have arbitrary shapes, and flakes of designed shape and sizes are favourable for some architectures. Pre-patterned graphene flakes have in particular been used for contacts to hBN-encapsulated TMDs, see Sec. 6.3.

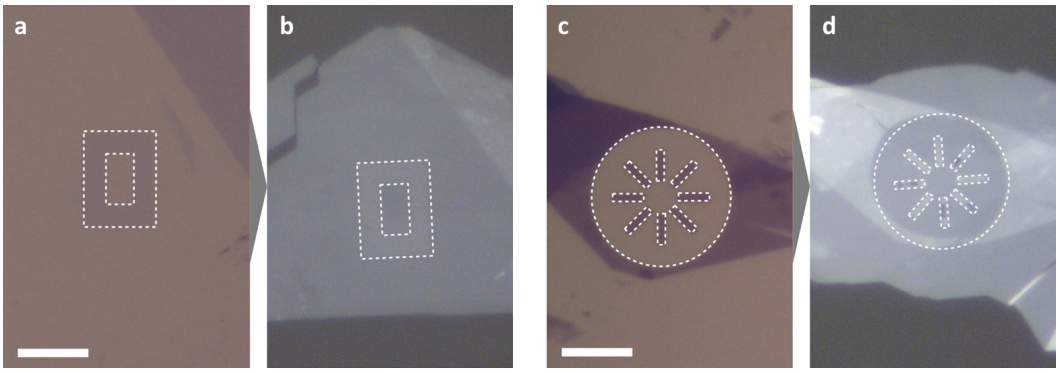


Figure 4.7: *(**a**) and (**c**) pre-patterned graphene on SiO_2. (**b**) and (**d**) pre-patterned graphene picked up on hBN. The scale bars are 5 µm. Published in [20].*

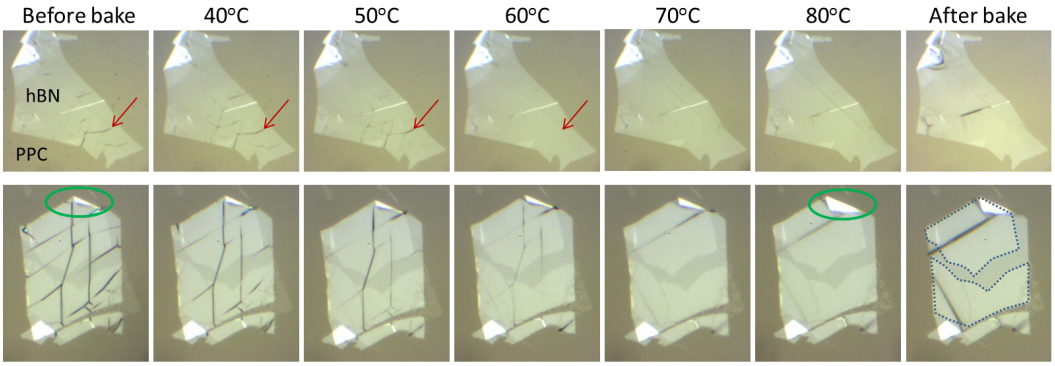


Figure 4.8: *Wrinkle removal by heating step II in Fig. 4.4. Top row: Images of a 6.2 nm thin hBN picked up with a PDMS/PPC slide. The wrinkles are gone after heating to 60 °C, the arrow indicates a wrinkle. Bottom row: 8.2 nm thin hBN after pick-up of a monolayer graphene flake. The lighter areas are hBN/graphene (indicated by dashed lines in the after bake image). The wrinkles are smoothened out at 70 °C, however the top corner of the hBN flake starts to fold on top of itself (indicated with a circle) when heating further.*

4.2.3 Step II: De-Wrinkle Bake

Picked up hBN flakes will often have optically visible wrinkles, which can be removed by baking. For thick flakes (thicknesses > 20 nm) a bake of 10 minutes at 110 °C is successfully used to remove wrinkles. Such a bake is not suitable for thin hBN flakes as these flakes tend to fold or roll up on themselves at temperatures above ~ 70 °C. Bakes of thin flakes are, in order to stop the bake when the flake has smoothened out, performed under the microscope at the stacking setup. Optical micrographs of the baking of thin hBN are seen in Fig. 4.8. The top row of images track the changes of a picked up hBN flake during a bake. The wrinkles are smoothened out at 60 °C, and do not reappear after cooling down to room temperature. Wrinkles are also present after pick-up of the second flake with the top-hBN flake, and can be removed in a similar way. Removal of wrinkles on hBN with graphene on top is shown in the bottom image row of Fig. 4.8. The graphene is indicated with a dashed line in the 'after bake' image. The hBN starts to fold onto itself when heated, and the overlap of the top corner is significantly increased at 80 °C compared to before baking. One explanation for this behaviour could be that the wrinkles are removed as the elevated temperature allow the hBN to smoothen itself out on the softer PPC.

4.2.4 Step III: Drop-Down

Drop-down refers to the action releasing a picked up flake(s) from the PDMS/PPC block on top of a target flake, see step III illustrated in Fig. 4.4.

The top-hBN is now to be dropped down on a graphene flake. A chip with exfoliated graphene is fixed on the vacuum chuck under the microscope with the heater at 110 °C. The glass slide is not held parallel to the chip during drop-down, but tilted to have more control over the movement of the PPC front at the elevated temperatures at which the PPC behaves more as a liquid.

The hBN on the PDMS/PPC block is aligned to the graphene on the chip, and the PDMS/PPC block is brought in contact with the surface of the chip. One side of the block will touch first as a result of the tilted slide. After creating contact the glass slide is lowered further to move the PPC front to the proximity of the graphene. This can be done relatively fast. The speed of the PPC front progressing over the hBN and graphene has to be very slow (< 1 µm/s) to squeeze out contaminants in-between the two flakes [20]. Movement of the PPC front can to

some degree be controlled by increasing the temperature further, making the drop-down very slow and continuous. The chip is kept at the high temperature for five to ten minutes after the flakes has been brought into contact to ensure good adhesion before releasing the hBN flake onto the graphene flake on the SiO_2 surface. The temperature is lowered to 70 °C for the release of the flake from the PDMS/PPC block. The glass slide is moved slowly up with the micromanipulator making the PPC front retreat while leaving the flakes behind on the chip, as illustrated in Fig. 4.4 Step III. The retreat of the PPC front should proceed slowly for a sucessfull drop-down.

Drop-down may also be performed at lower temperature, which may be preferred for air sensitive TEMs and thin top-hBN flakes as these tend to fold up on them self at high temperatures. It is possible to obtain a clean interface at a low temperature drop-down; however it is more difficult and will require an even slower squeeze out.

4.2.5 Step IV: Adhesion Bake

The chip will be baked after drop-down to promote the adhesion between the two stacked flakes before picking them up to continue the heterostructure assembly. The bake will reveal any contamination trapped between the flakes, as the contaminations accumulate to form bubbles/blisters, through the same temperature-enhanced squeeze-out mechanism as described in Sec. 4.2.4 as well as in literature [78]. These are visible optically especially in dark field. Bakes of 170 °C are used. Bubbles are unwanted as they deteriorate the transport properties and because they compromising the van der Waals interlayer adhesion between the flakes, making subsequent pick-up difficult. Stacking heterostructures at high temperature reduces interfacial contamination and thereby bubbles/blisters [20].

The four steps are repeated to pick-up the hBN/graphene and drop them down on the bottom-hBN for fully encapsulating the graphene, see lower part of Fig. 4.4. For more complex heterostructures with more flakes, the cycle of pick-up and drop-down is simply repeated for all the flakes until the desired heterostructure is completed. The risk of failure is naturally increasing with the number of flakes assembled even though the pick-up yield can approach close to 100 %. The main reason for failure during pick-up and drop-down is rupturing of flakes and folding of flakes, respectively.

Batch fabrication of van der Waals heterostructures is feasible with the hot pick-up method presented here [20], as the four stacking steps allows for stacks to be assembled in parallel. By doing so time is not only saved at baking and rinsing steps, but also in the subsequent fabrication process of lithography steps.

4.2.6 van der Waals Interaction

The Lennard Jones potential describes how the potential energy relate to the short-range Pauli repulsion and the long-range attractive vdW forces act between two uncharged particles separated by a distance, r

$$E_{LJ} = \frac{C_{rep}}{r^{12}} - \frac{C_{vdW}}{r^6} \ . \tag{4.1}$$

The vdW forces between atoms/molecules have three contributions, the Keesom forced due to the attraction between two permanent dipoles, the Debye forces between a permanent dipole and an induced dipole, and finally the London dispersion force. London dispersion force arises from quantum mechanical fluctuations in the charge distribution in an atom or a molecule. The electrons of a molecule will be redistributed in proximity of another molecule, inducing dipole moments that in average over time lead to a net attraction.

Figure 4.9: *Illustration of vdW interaction forces for corrugated monolayer and rigid multilayer 2D flakes to a SiO_2 substrate. Inspired by figure by Peter Bøggild.*

For vdW assembly of 2D crystals the vdW energy between two flat surfaces is of interest. The interaction between two arbitrary shaped bodies can be approximated by the Hamaker method, where the vdW force is simply summed up for all pairs of atoms in the two bodies, implying that the these pair-pair interactions are independent on the presence of other atoms making out the solid. The vdW energy per area between to flat surfaces separated by a distance, D, is

$$E = \frac{-A_H}{12\pi D^2} \ , \tag{4.2}$$

where $A_H = C_{vdW}\pi^2\rho_1\rho_2$ is the Hamaker constant. Here, C_{vdW} is the interaction parameter for the particle-particle pair interaction and $\rho_{1,2}$ is the number density of atoms per unit volume in the two materials.

Whether a flake is picked up or left behind on the SiO_2 surface depends on which of the interfaces is held together by the largest adhesion forces. SiO_2 have a rough surface compared to that of mutilayer 2D crystals [24]. The rigidity of the 2D flakes depend strongly on the thickness [48]. Monolayer graphene conforms more to the rough surface compared to bilayer and multilayer flakes. The corrugation of monolayer graphene becomes comparable to that of the SiO_2 if the graphene is exposed to heat treatment [46], see also AFM scans of Fig. 5.2. The vdW forces between monolayer graphene and the SiO_2 surface will therefore be larger compared to thicker graphene flakes. Thicker flakes will, due to their rigidity, not conform to the surface, and will therefore have an smaller effective contact area of vdW interaction with the SiO_2 surface. This lead to a low adhesion between the thick flake and the SiO_2 compared to thin flakes, thick flakes are therefore more easily picked up, see illustrations in Fig. 4.9.

The PPC used for the pick-up is heated above its glass transition temperature to get it to conform to the flake and thereby have a higher adhesion between the PPC and the flake, then between the flake and the substrate. This is not possible for the thin flakes, as these adhere very well to the substrate. Pick-up of thin flakes is only possible with another 2D flake. The adhesive bake have experimentally shown to increase the yield of the pick-up of especially monolayer graphene. The bake is assumed to increase the adhesion between the flakes, as it is more energetic favourable for the thin flake to conform to the flat surface of the hBN compared to the rough SiO_2 surface. For the vdW assembly to work it is important with an atomically clean interface which is obtained with the high drop-drown temperatures. If there is contamination in-between the two layers the adhesion will be strongly diminish as the vdW forces depend strongly on the distance.

4.3 CAB Transfer

The van der Waals stacking method is not applicable for thin and monolayer flaks, as thin flakes both are difficult to pick-up and they tend to curl up on the PPC when heated. Cellulose acetate butyrate (CAB) wedging transfer [79] is a recommendable and robust technique of transfer of flakes of all thicknesses. The steps of the CAB transfer are illustrated in Fig. 4.10. For this

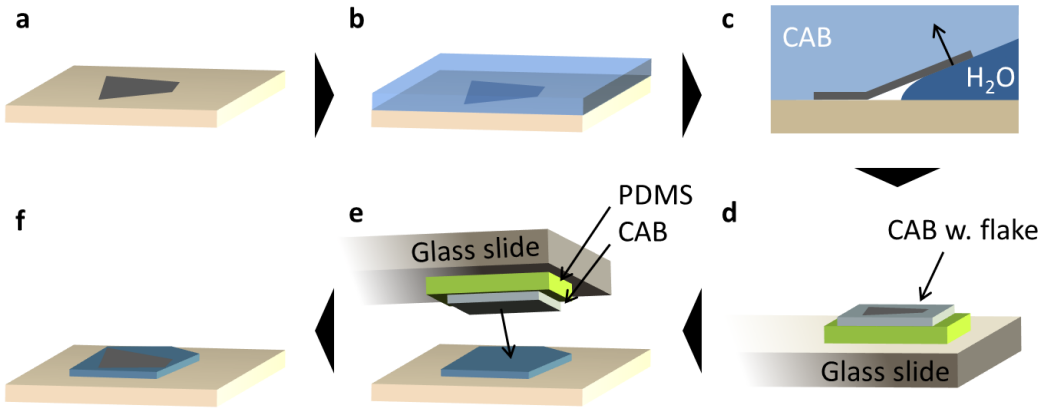


Figure 4.10: *Step wise illustrations of the CAB transfer technique. (**a**) Flake on initial substrate and (**b**) after CAB is spun on the chip. (**c**) Water is used to lift the CAB and flake of the SiO_2 substrate by wedging. (**d**) CAB with flake are placed on a PDMS block attached to a glass slide for alignment with the micro-manipulator at the vdW microscope setup. (**e**) The CAB and flake is aligned and places onto the target substrate, in this case an other flake. (**f**) The flakes after transfer the CAB is rinsed of in ethyl acetate, acetone and IPA.*

transfer, a solution of 30 k CAB dissolved in a 30 g/100 mL ethyl acetate is spun on the chip at a speed of 1000 rpm, acceleration of 200 rpm, and baked at 75 °C for half an hour. A cut is made with a scalpel in the CAB around the flake being transferred, a drop of water is placed at the cut, causing the water to wedge in-between the SiO_2 and the CAB gently lifting the CAB and flakes off the substrate, Fig. 4.10c.

The CAB can either be aligned by moving the CAB with tweezers while having a droplet of water between the CAB and the target substrate, or by letting the CAB dry and then place it on a glass slide with a PDMS block, as illustrated in Fig. 4.10d. The micro-manipulator can then be used to align and drop the CAB and flake on the target substrate. The sample is baked for half an hour at either 80 °C for uniform samples or 135 °C, which is above the glass transition temperature of the CAB, for very non-uniform surfaces. This bake is performed to ensure good adhesion between the transferred flake(s) and the target substrate. The high temperature bake should be avoided if possible as this leads to an extended amount of residues. Finally, the sample is rinsed thoroughly in ethyl acetate, acetone and isopropyl alcohol (IPA) to remove the CAB.

CAB transferred flakes will be in direct contact with various solvents, water and CAB. Furthermore, water may be trapped under the flake, and the CAB will to some extend leave residues on the surface of the flake. Hence this technique is far from as clean as the pick-up method, but it can be used for some of the transfers where the pick-up method is not applicable. The CAB technique is very feasible for transfer of graphite top gates to stacks after fabrication, whereas the drop-down of the vdW assembly is difficult on the non-uniform surface. CAB has also been used for transfer of graphene to TMDs to use the graphene as intermediate contacts, as the thin graphene cannot be picked up by the vdW assembly technique. Furthermore, for the sensitive TMD flakes the bake at 80 °C may be replace with a few minutes bake under the microscope at temperatures below 50 °C. The short bake increases the risk of failure but not strongly, approximately one in five transfer wailed when the 80 °C bake was omitted.

4.4 Device Fabrication

2D flakes are arbitrarily shaped and randomly distributed after exfoliation. Device architectures must therefore be costume-made for each flake/stack, hence, electron beam lithography (EBL) is optimal for fabrication and has been widely used in this project. However, EBL is also rather time consuming and stencil lithography may therefore be used as a clean and fast alternative for testing and optimisation of fabrication steps. Both lithography techniques are described in this section. Fabrication boxes throughout the thesis outline the specific fabrication of devices in their dedicated result chapters. The different steps are in the fabrication boxes listed with side-view illustrations and typical parameters for the process.

The design of single flakes on SiO_2 is often rather simple. The flake will be contacted with metal deposited on top of the flake, and possibly be etched into a desired shape. For stacks, the designs may be more complex. Especially the design requirement for 1D contacts to hBN encapsulated graphene depends strongly on the full device architecture. For instance, in top gated devices, the metal on the contacts should not cover the stack as it will screen the gating of the graphene under the contact. Moreover, in devices with graphite back-gate, the contacts have to be made without etching the bottom-hBN as this will lead to short-circuiting of the device and the gate. Selective etches and three variations of the 1D contacts have been developed and investigated to meet these demands.

4.4.1 Stencil Lithography

Stencil lithography is a fast, clean and simple device fabrication technique where contact with polymers, chemicals and heat treatment can be avoided [46]. Stencil devices are here made by aligning the cross-bars in commercially available TEM grids on top of the flake [50, 80, 81, 82].

Stencil contacts are fabricated by first aligning the TEM grid shadow/stencil mask to the flake under an optical microscope and then fixing the grid with Kapton ® Tape to the SiO_2 surface. Metal is then deposited by electron-beam evaporation through the stencil. The TEM grid is gently removed and the device is ready for electrical measurements. The stencil device channel covered by the mask is left in a pristine state, making stencil devices ideal as a diagnostics tool for process optimisation and for fast prototyping.

4.4.2 Electron Beam Lithography

Two E-Beam systems have been used: a 100 keV JEOL JBX-9500FS and a Raith Elphy system installed in a Leo 1550 SEM.[1] Two positive E-Beam resists, polymethyl methacrylate (PMMA) from Sigma-Aldrich and AR-P 6200 (CSAR 62) from ALLRESIST, have been employed.

CSAR 62 is used for fabrication of index marks on 4-inch wafers, since this reduces the writing time as CSAR 62 requires a lower dose ($\sim$1/3 compared to the dose for PMMA). PMMA is used for all device fabrication, where the writing time generally is short. A 4 wt% solution of 996K PMMA dissolved in anisole is used for standard shaping and metal leads to flakes/stacks. Before spinning PMMA the sample is given a 10 minutes dehydration bake at 180 °C to ensure a good adhesion between the PMMA and SiO_2 surface [83]. The 4 wt% PMMA is spun at a speed of 1500 rpm and an acceleration of 500 rpm for 1 min to obtain a thickness of 200 nm-250 nm. Finally the solvent is baked out with a 10 minutes bake at 180 °C directly after spinning.

For EBL steps followed by both etch and metal deposition, a bilayer PMMA is used to improve the metal lift-off. The bottom layer contains a low molecular weight PMMA (8 wt% PMMA 25K in anisole) and the top layer contains a high molecular weight PMMA dissolved in

[1] I have been responsible for EBL in the JEOL JBX-9500FS and co-worker Bjarke Sørensen Jessen have been responsible of EBL carried out in the Raith Elphy system.

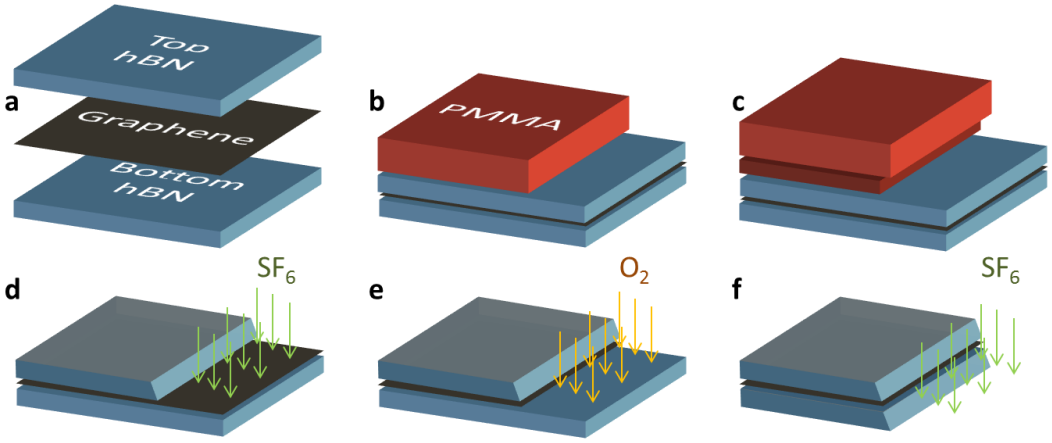


Figure 4.11: *(**a**) Illustration of hBN/graphene/hBN stack. Sketch of developed (**b**) monolayer PMMA and c) double layer PMMA. (**d-f**) Etching process of a hBN/graphene/hBN stack. The SF_6 etch is used to etch the hBN and the O_2 etch is used for the monolayer graphene, which works as a hard mask for the SF_6 etch.*

methyl isobutyl ketone (MIBK) (2 wt%-4 wt% PMMA 996K in MIBK). PMMA is less dissolvable in MIBK, and MIBK is therefore used for the top layer to reduce the dissolution of the first layer when spinning the second PMMA layer. The bilayer PMMA results in an undercut in the resist side-wall profile after development as the dissolution rate is larger for the lower molecular weight PMMA, see Fig. 4.11c.

PMMA is a high resolution resist and is also used for dense nano-structuring of hBN-encapsulated graphene. Triangular antidot lattices of periods down to 35 nm have been fabricated in devices and defect free structures with periods down to 30 nm have been made in hBN, see Sec. 5.3. A thin PMMA layer is needed to have a suitable aspect ratio with the nano-pattern density. Generally a 2 wt% PMMA 996 K solution in anisole is used to get a thickness of $\sim$ 50 nm (spun at 3500 rpm acc. 500 rpm, 1 min).

4.4.3 Etch of 2D Crystals

In much published work, a universal etch is used to etch the whole stack of flakes in the device. These etches either have a chemistry of fluorine and oxygen or fluorine and argon – the later making the etch more physical [21, 23, 73]. We have developed one etch for graphene and one for hBN and TMDs. Both etches are performed in an SPTS ICP Etcher. The graphene is etched with a mixture of oxygen and argon. Flow rates of 5/15 sccm for O_2/Ar, pressure of 80 mTorr and a coil/platen power of 0/20 W are used for the etch. TMDs and hBN flakes are etched with a sulfur hexafluoride (SF_6) based etch. Flow of 40 sccm SF_6, pressure of 80 mTorr and a coil/platen power of 0/75 W are used. The etches are highly selective which especially is important for nano-patterning, as the thin PMMA layers, which are required for fabrication of dense nano-patterns, have to withstand the etching needed to transfer the EBL defined pattern into the device. Fig. 4.11d-f illustrates the etch of a hBN/graphene/hBN stack, where three etch steps are applied (SF_6 + O_2 + SF_6) to etch the top-hBN, graphene and bottom-hBN, respectively. Etch rates for the two etches are listed in Table 4.1 for relevant materials.

Monolayer graphene is not etched by the SF_6-based etch, and graphene can therefore work as a hard mask/etch stopper when etching stacks. The graphene exposed to the SF_6 etch is not unchanged, but becomes fluorinated [84, 85]. The fluorination is further studied with electrical measurements and Raman spectroscopy in Sec. 5.1.3.

AFM and SEM inspections have here been used to analyse the etch of hBN flakes. The

Table 4.1: *Etch rates in graphene, hBN, PMMA and SiO_2 for the highly selective O_2/Ar and SF_6 etch processes. O_2/Ar is used for etching graphene, and SF_6 is used for hBN and TMDs.*

Material	O_2/Ar etch [nm/min]	SF_6 etch [nm/min]
Graphene	~15	0
hBN	0	~400
PMMA	80	31
SiO_2	0	7

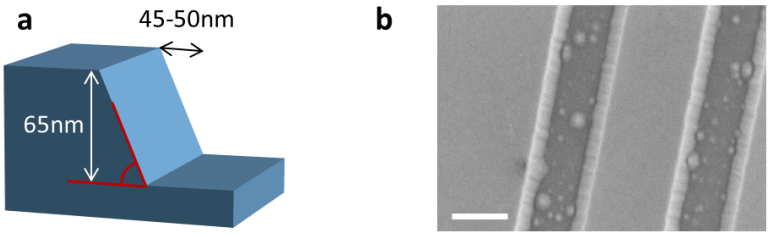


Figure 4.12: *(**a**) Illustration of the etch profile in hBN. The dimension are obtained with SEM and AFM inspection and the marked angle is 53.9° ± 1.5°. (**b**) SEM micrograph of trench etched into a hBN flake, the scale bar is 200 nm.*

hBN flakes are not etched vertically but at an angle of 53.9 ° ± 1.5 °, as illustrated in Fig. 4.12. The etch angle makes the nano-patterning of hBN-encapsulated graphene challenging, as very thin top-hBN are needed to transfer a dense nano-pattern through the hBN into the graphene.

4.4.4 Metal Deposition

Various electron-beam evaporation systems have been employed for metal deposition of electrical contacts to 2D flakes on SiO_2 and hBN-encapsulated graphene. For 2D flakes on SiO_2, mainly contacts of pure 50 nm Au or 5/50 nm Cr/Au have been deposited on top of the flake. For hBN-encapsulated graphene 1D metal contacts of 2/15/30 nm Cr/Pd/Au or 2/50 nm Cr/Au are used following the suggested metal combination from the first 1D edge contacts from [21]. Most depositions are performed at low pressure (below $2 \cdot 10^{-7}$ mbar for the Cr layer) and with low deposition rates (approximately 1 Å/s for Cr and Pd and approximately 3 Å/s for Au). Deposition are performed in a Physimeca ΦSES250 electron-beam evaporation system.

4.4.5 One-Dimensional Contacts

Three variations of one-dimensional contacts to hBN-encapsulated graphene have been employed depending on the device requirements. Firstly, the architecture presented by L. Wang *et al.* [21] have been used. These contacts are made by first shaping the stack into the desired shape, by EBL and etching, see Fig 4.14a-b. A second EBL step is then performed to define the metal contacts and leads, Fig 4.14c-d. The contacts are designed with an overlap onto the stack to ensure contact even with a slight misalignment between the two EBL steps, see schematic in Fig. 4.13a. A disadvantage of the overlap is that a potential top gate will not be able to gate the graphene under the metal contact overlap, as the metal will screen the gate. Examples of these contacts are seen in the devices of Sec 5.2.1, where also fabrication Box 2 illustrate the fabrication process.

A second type of 1D contacts was developed to have a zero overlap onto the stack, see Fig.

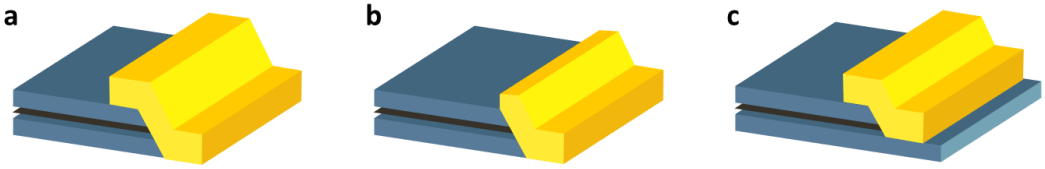


Figure 4.13: *Sketch of three designs of 1D contacts to graphene encapsulated in hBN, (**a**) standard 1D contacts, first demonstrated in [21] (**b**) one step 1D contacts with zero overlap onto the stack, ideal for top gating, (**c**) 1D corner contacts where only the top-hBN and graphene is etched, ideal for graphite back-gates.*

4.13b. These contacts are made with one EBL step where the leads are defined first, the SF_6 + O_2 + SF_6 etch is performed and metal is deposited directly after the etch. A bilayer PMMA, as sketched in Fig. 4.11c, is used to ensure good lift-off after etch and metal deposition. A second EBL step can be performed to shape the stack. The one-step 1D contacts have in principle zero overlap with the stack and are therefore good for top gated devices, and thus short channel transistors. They may also be used to make graphene devices without exposed edges.

Finally, 1D corner contacts were designed for devices with graphite back-gates. For these contacts only the top-hBN and graphene is etched, see Fig. 4.13c. The selective etching is possible as even a monolayer of graphene works as a hard mask for the SF_6 based hBN etch described in Sec. 4.4.3. This fabrication method is sensitive to cracks in the graphene, as a crack will lead to the etch reaching the graphite back gate. If the crack is under a metal lead, this will lead to a leakage current between the gate and device. To minimise the likelihood of gate leakage only a small part of the stack is etched where the metal leads will get in contact with the graphene, and the leads are then lead up on top of the stack and away from the device. This type of contacts has been used for the devices of Sec. 5.3, see fabrication Box 3.

It has not yet shown possible to obtain a good contact to hBN-encapsulated TMDs with 1D edge contacts, and intermediate graphene contacts are therefore used to contact these. See Sec. 6.3 and fabrication Box 5 for details.

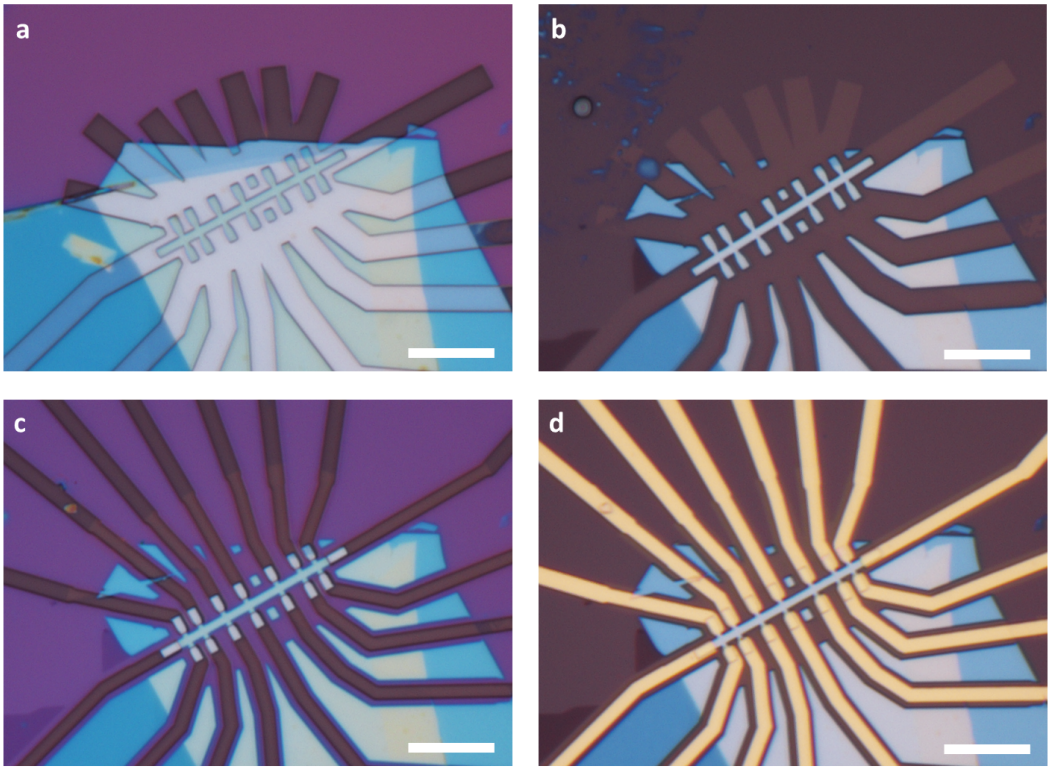


Figure 4.14: *Fabrication steps from assembled stack to contacted device. Optical micrograph of stack (**a**) after E-beam exposure and development for the shaping step and (**b**) after etching with SF_6 and O_2. (**c**) Shaped device with exposed and developed E-beam resist for metal leads and (**d**) after metal deposition of Cr/Pd/Au and lift off in acetone. Scale bars are 10 μm.*

5 Graphene

This chapter covers the results from graphene stencil devices and devices of hBN-encapsulated graphene. The fabrication of stencil devices is quick and clean, and the devices are therefore ideal as a diagnostic tool for process optimisation and testing. Graphene stencil devices have here been used for testing the influence of processing with PMMA, heating and SF_6 etching. Furthermore, electrical characterisation of hBN-encapsulated mono-, bi- and trilayer graphene devices fabricated with the "Hot pick-up" method, and devices of dense nano-patterned hBN-encapsulated graphene with graphite back-gates are presented.

Contents

5.1 Graphene Stencil Devices

Graphene, consisting entirely of surface atoms, is highly influenced by the environment. Graphene on SiO_2 is not only influenced by the substrate and ambient air but also by processing involving heating, polymers and chemicals, whereas hBN-encapsulated graphene to a large extent is

shielded from the environment. Hence, before the development of van der Waals heterostructures device architectures, it was difficult to avoid contamination from the fabrication processes to get in direct contact with the device channel.

The evolution of graphene's electrical transport properties due to processing with the polymer PMMA and heating are examined with graphene stencil devices in Sec. 5.1.1 and Sec. 5.1.2. These two sections are based on the work published in [46] (2014 L. Gammelgaard, *et al.*). Heating generally promotes conformation of graphene to SiO_2 and is found to play a major role for the electrical properties of graphene while PMMA residues are found to be surprisingly benign, leading mostly to temporary and reversible changes. Graphene stencil devices are likewise used to test the impact of the SF_6 etch step used to etch hBN and TMDs, see Sec. 5.1.3. Electrical measurements and Raman spectroscopy on graphene stencil devices are used in parallel to evaluate the impact of the SF_6 etch on the graphene.

The fabrication of stencil devices is both fast and clean, as it is a one step process and no solvents or polymers are involved. The steps from an exfoliated flake to a contacted device are outlined in Box 1 with illustrations.

Box 1: Stencil device

Fabrication steps from a pristine flake to stencil contacted device.

Illustration	Step	Parameters
	Mask alignment	Stencil mask is aligned to the flake under an optical microscope Mask fixed with Kapton ® tape
	Metallisation	50 nm Au or 5/50 nm of Cr/Au
	Mask removal	Kapton ® tape and stencil mask are removed with tweezers

5.1.1 Influence of Processing with PMMA

The influence of processing with PMMA is of great interest, as PMMA is not only used as an EBL resist but also for a large part of published transfer techniques [86, 87, 88]. PMMA invariably leaves residues on graphene after being in direct contact. This is considered to be a serious problem for device fabrication, as PMMA residues are notoriously difficult to remove [89, 90]. Furthermore, processing with PMMA typically implies temperature annealing steps in controlled atmospheres and/or baking in air [83, 91, 92], which also tend to impede the device performance.

The evolution from the pristine monolayer graphene to the PMMA processed graphene is here evaluated by measuring the electrical properties of the stencil devices after each individual processing step on stencil devices. Electrical measurements were undertaken after each of the following stages: (1) After stencil device fabrication, where the device is considered to be as close to its pristine conditions as possible. (2) After 30 minute temperature anneal at 250 °C in a nitrogen atmosphere (TA). (3) After ventilation of the device chamber with ambient air. (4) After baking at 200 °C in air for 30 minutes (both time and temperature are typically used in EBL fabrication as a dehydration bake [83]). (5) After applying, curing and removal of a 40 nm

thick PMMA layer. The PMMA was spun and cured on the devices using a temperature ramp typical for high resolution EBL [91]. The curing process starts with a one hour temperature ramp from room temperature to 120 °C. The devices were then held at this temperature for three hours, before being ramped to 180 °C over one hour, and held at this temperature for six hours, followed by a ramp back to room temperature over two hours. The curing process was carried out in ambient conditions. The PMMA was removed in 40 °C acetone and the devices were rinsed in isopropyl alcohol (IPA) before a N_2 dry. After these process steps PMMA residues were clearly present on the graphene, as seen in the SEM image in supplementary Fig. S.2 of [46]. (6) Finally, electrically measurements after temperature anneal of the devices as in step 2, which is a common step carried out to enhance the electrical properties of graphene devices [66, 89, 93, 94]. The six fabrication steps are sketched in Fig. 5.1a along with field-effect measurements for device D1 in Fig. 5.1b.

Regarding the evolution of the electrical measurements, the key figures of merit (FoM) for this study is the average position of the charge neutrality point V_{CNP}, the gate voltage hysteresis ΔV_{CNP} and the mobility. The mobility is represented by the hole carrier mobility μ_h, as the devices become highly p-doped at some of the process steps. V_{CNP} and ΔV_{CNP} are found directly from the gate voltage sweep. The value for μ_h is more challenging to determine in the two-terminal graphene devices due to the contact resistance of the source and drain contacts R_C. The model presented in Sec. 2.4.1 is applied to the data in order to extract μ_h. The evolution of the three key FoM, ΔV_{CNP}, V_{CNP} and μ_h, of the graphene along with the six processing steps is plotted in Fig. 5.1c-e.

The gate voltage hysteresis, ΔV_{CNP} in Fig. 5.1c, is largest for the measurements of the initial as-fabricated devices (step 1). A smaller hysteresis is also present after ventilation of the chamber (step 3), and after PMMA processing (step 5). Thermal annealing in a N_2 atmosphere and baking in air (step 2, 4 and 6) considerably reduced ΔV_{CNP}. Hysteresis in graphene devices is commonly ascribed to adsorbed water molecules and other species [80, 66]. In our case the large initial hysteresis could be due to presence of water below as well as on top of the graphene after fabrication [95]. The amount of water below the graphene and thereby the hysteresis can be minimised with the use of a hydrophobic substrate [51, 94, 96, 97]. After the first TA water will mainly be re-adsorb on top of the graphene, leading to a smaller increase in hysteresis when again exposing to air. Another possibility is that the first annealing step desorbs a considerable amount of non-water species that contribute to the higher initial hysteresis, and which do not all readsorb upon air exposure.

The evolution of doping level, V_{CNP}, Fig. 5.1d, follows the same trend for all the devices after the first temperature anneal. A large variation of the initial V_{CNP} was observed in the as-fabricated devices (step 1), which corresponds to a spread in charge carrier concentration of $\Delta n \sim 4 \times 10^{12}\,\mathrm{cm}^{-2}$ among the measured devices. Similar variations of n on exfoliated non-processed graphene on SiO_2 have been extracted via Raman spectroscopy [98, 99, 100]. After the sequence of PMMA processing steps, involving chemicals and heating, p-type doping with a smaller variation is measured on all the devices. The hole carrier mobility μ_h is shown in Fig. 5.1e. Similar to V_{CNP} a large initial spread of μ_h (from $2000\,\mathrm{cm}^2/\mathrm{Vs}$ to $8000\,\mathrm{cm}^2/\mathrm{Vs}$) was observed in the as-fabricated devices, which however decreased with the number of processing steps.

As explained in detail below, both the p-doping and carrier mobility behaviour is attributed as an interplay between particle contamination and the mechanical conformation of the graphene to the substrate due to processing steps particularly involving heating.

On one hand it is known that the presence of molecules on graphene strongly affect the charge carrier concentration of the monolayer. In particular O_2 molecules together with H_2O molecules lead to strong hole doping of graphene [50, 51, 52]. On the other hand, the mobility is influenced by the substrate in two ways. First, contact with SiO_2 leads to polar optical phonon scattering [36, 101]. Second, the higher the conformation of the graphene to the

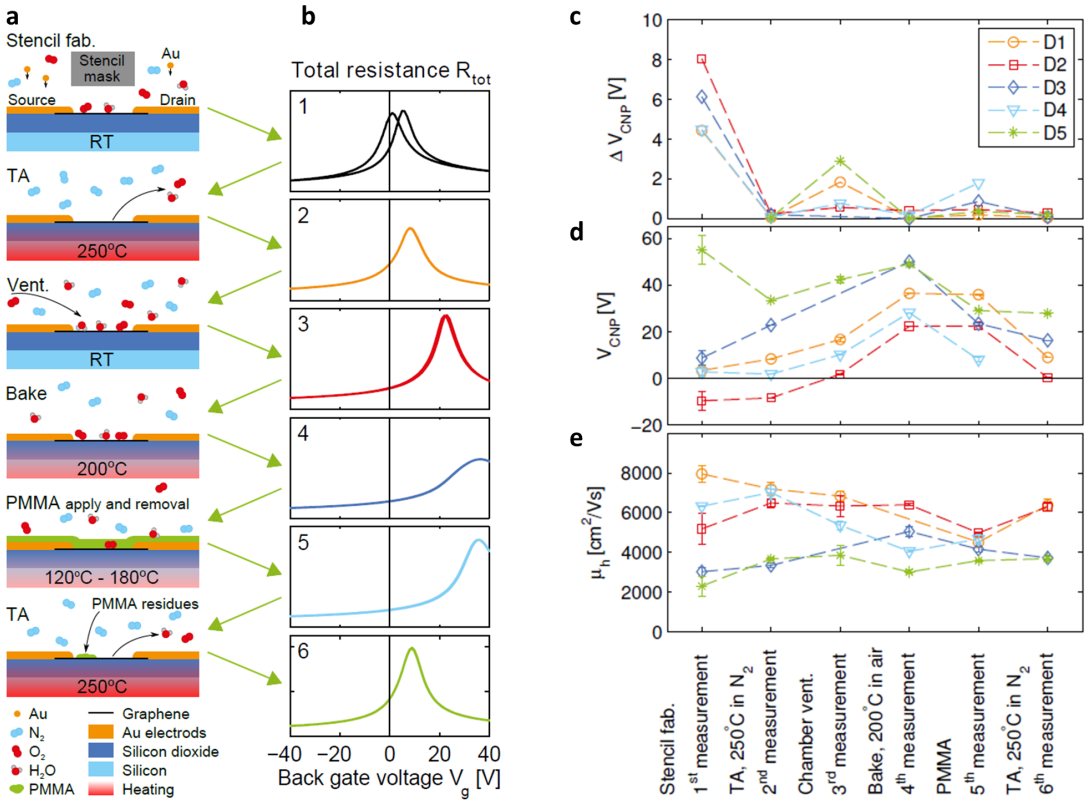


Figure 5.1: *(**a**) Outline of the process steps and (**b**) field-effect measurement performed after each step on the representative device (D1). All y-axes are scaled from 0 kΩ to 4.5 kΩ. The evolution of the (**c**) gate voltage hysteresis ΔV_{CNP}, (**d**) the doping V_{CNP} and (**e**) the hole mobility μ_h throughout the six selected PMMA processing steps, for the five studied devices. All electrical measurements are performed at room temperature in a N_2 atmosphere at ambient pressure. All devices are made on highly doped (1-2 mΩ · cm) silicon wafers with 300 nm SiO_2, and the contacts are made of 50 nm Au. Published in [46].*

corrugated SiO_2 substrate, the larger is the reactivity of the graphene towards oxygen molecules [50]. A higher conformation to the SiO_2 substrate would therefore lead to an increase of the amount of impurities on the graphene, which in turn reduces the carrier mobility through long-range Coulomb scattering [102] and increases the doping level of the graphene [50, 102]. In agreement with this picture, graphene has been reported to be far more smooth on exfoliated hexagonal boron nitride substrates than on SiO_2, without the distinct p-doping upon exposure to air [24, 103, 104]. Furthermore, according to [50] and [104], graphene conforms more to the substrate when it is heated up. To confirm this for the stencil samples, line scans were carried out across the graphene-SiO_2 interfaces using AFM, and compared directly regions before and after annealing. Before annealing, Fig. 5.2a, c, the graphene flake appears qualitatively different from the SiO_2 surface, with clear lateral streaks, as also reported in [98], yet with significantly less vertical corrugation. It is noted that the graphene flakes before annealing appear to conform to the SiO_2 near the edges. After annealing the graphene and SiO_2 surface appear strikingly similar except for a vertical offset. The scale of vertical corrugations on graphene and SiO_2 is very similar after annealing. Care was taken to perform the line scans in the exact same position, and the curves before (blue) and after (black) annealing show nearly the same features on the SiO_2.

In the electrical measurements, after the first TA in step 2, as-fabricated graphene conforms

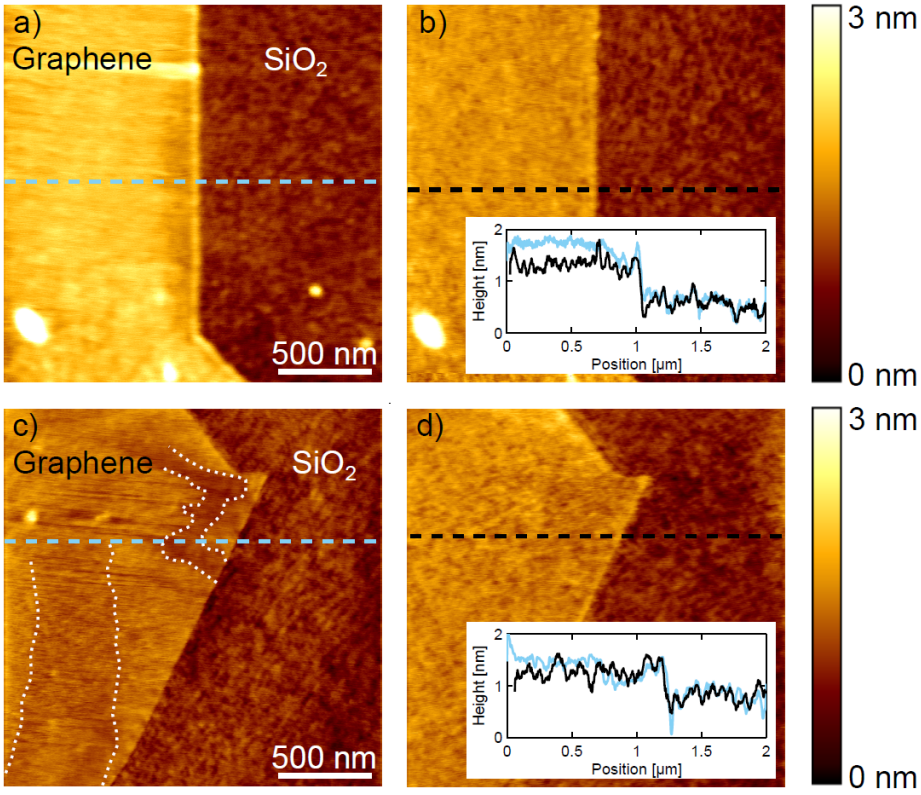


Figure 5.2: *AFM micrographs of two graphene flakes (**a**) and (**c**) before and (**b**) and (**d**) after heat treatment. The line scans were extracted in approximately the same position, which is apparent from the insets, showing before and after annealing curves as blue and black color, respectively. Before annealing the graphene flakes show extended ripple-like texture, very different from the SiO_2 surface, and overall smaller vertical corrugations from the oxide. After annealing the surfaces clearly resemble each other, and have similar surface roughness. The white dotted line in panel (**c**) marks areas with pronounced micrometer sized corrugations. Published in [46].*

more to the SiO_2 surface, which does indeed support the interpretation of the observed p-doping in all the devices upon ventilating the chamber (step 3). This behaviour was consistently observed in all devices studied here, as well as any other devices investigated prior to this study (>20). Furthermore, this rapid doping was confirmed by Raman spectroscopy. Raman spectra were obtained through a glass window in the environmentally controlled Linkam measurement chamber, in which a pristine graphene flake first was thermally annealed at 250 °C in nitrogen and then slowly exposed to ambient air while collecting Raman spectra, see Fig. 5.3. The G peak position before annealing was 1585 cm^{-1} and the FWHM was 14 cm^{-1}. The Raman data presented in Fig. 5.3 confirms that the samples are getting doped due to exposure to air upon temperature annealing. The G peak shifts from 1583 cm^{-1} to 1588 cm^{-1} and the FWHM of the G peak also decreases. This indicates that the initial doping (before annealing) was significantly lower than the level achieved after the re-exposure to air. This behaviour is explained by the higher reactivity introduced by the higher conformation of the graphene to the substrate after annealing.[1] The devices are also observed to become further p-doped after the bake in air at step 4. The possibility of recovering the original FoM of graphene upon baking in air is investigated further in Sec. 5.1.2.

[1]Raman characterisation was performed in a DXR Raman Microscope from Thermo Scientific with a 455 nm excitation laser by Alberto Cagliani

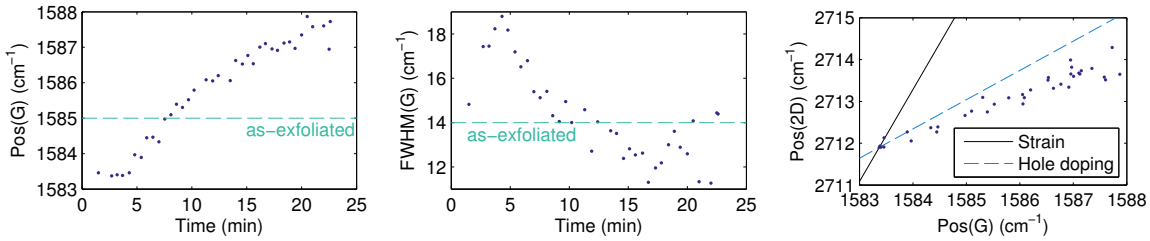


Figure 5.3: *FoM from Raman spectra of graphene after re-exposure to air upon a temperature anneal of 250 °C in nitrogen. At t = 0 min the nitrogen flow is turned off allowing ambient air to slowly enter the device chamber while recording optical Raman spectra. (left) Position of G peak as function of time after exposure to air, (middle) FWHM of the G peak, (right) Position of the G peak versus position of the 2D peak along with the expected relation between the two as a result of strain and hole doping [105]. Published in [46].*

The same explanation as for the doping behaviour also holds for the observed changes of μ_h. The devices with a high initial μ_h (D1 and D4) would have a lower degree of conformation to the substrate and following the argument presented above, a lower level of impurities on the graphene surface and lower coupling to the phonons of the SiO_2. After the TAs and baking in air are performed, the conformation of the graphene to the SiO_2 is increased, and the level of charged impurities is consequently enhanced. This leads to phonon and Coulomb scattering and a decrease in the value of μ_h. In contrast, devices with an initially high conformation of the graphene to the SiO_2 would have a low initial μ_h. This latter case represent the commonly observed electrical features from conventionally contacted devices, where graphene already is conformed during the lithographic steps and any annealing process carried out afterwards mainly improves the performance of the devices [92]. This trend is observed in D3 and D5 after the corresponding annealing processes. It is also noted that after the full sequence of processing steps, the devices have a more uniform value of μ_h, similar to devices contacted using conventional lithography [66]. In addition, the carrier mobility of the devices is not consistently modified after the PMMA exposure step, which shows that the sole presence of PMMA on top of graphene cannot alone be held responsible for degrading the mobility of graphene on SiO_2, at least not for devices in this quality range.

Finally, it is noted that the devices only after all the PMMA processing steps have the typical characteristics of Coulomb scattering [102], where the devices with lowest doping have the highest mobility and vice versa. This trend was not observed in the as-fabricated graphene devices, due to the interplay between the variation in the degree of conformation to the SiO_2 substrate and the amount of impurities on the monolayer. This work elucidates the evolution of electrical characteristics evolution during the chemical and heating typical from PMMA processing reconciles optical Raman measurements of unprocessed graphene [98, 101, 106] and electrical measurements on devices contacted by standard lithographic techniques [66, 102].

5.1.2 Influence of Heating under Ambient Conditions

Stencil devices are in this section used to test the possibility of baking graphene on SiO_2 under ambient conditions without permanently diminishing the electrical properties. Baking in air on hotplates or in ovens are commonly performed in cleanroom processing as a dehydration bake to evaporate water from the surface of the wafer prior to EBL- or photo-resist application [83]. As baking of graphene in air at 200 °C turned out to contribute to the p-doping during the PMMA processing steps, this step was investigated further to determine the baking temperature up to which doping and mobility degradation are still reversible by temperature annealing.

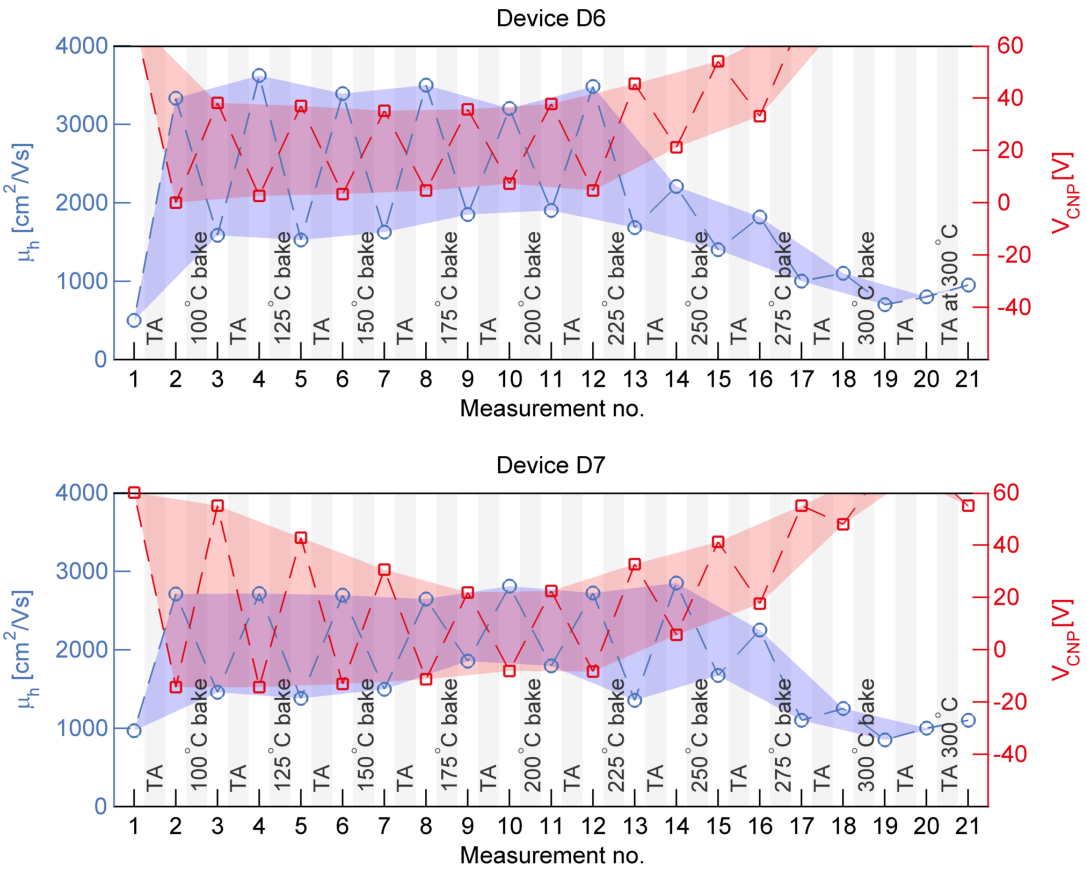


Figure 5.4: *The evolution of the charge carrier mobility (left y-axis and ○) and doping level (right y-axis and □) of two stencil devices, that are alternated between bakes in air and temperature annealing in nitrogen. All the electrical measurements are performed at room temperature in a N_2 atmosphere at ambient pressure. Published in [46].*

The enhancement of the electrical properties of graphene by temperature annealing in vacuum have shown to increase with annealing temperature until a turnaround temperature, after which the electrical properties start to diminish [107]. We observe the same trend for temperature anneals in N_2 on the stencil samples. The annealing temperature is therefore fixed to obtain the same values of doping and mobility after repeating TA on graphene devices. All temperature anneals (unless otherwise stated) lasted 30 minutes and were performed at 250 °C in N_2. The first temperature anneal immediately leads to an enhanced conformation of the graphene to the substrate before baking in air and thus increasing the reactivity with air species [50, 104, 108].

The stencil devices were first measured in their initial as-fabricated state (meas. 1 in Fig. 5.4), followed by temperature annealing to determine the baseline electrical characteristics of the devices (meas. 2). The devices were then repeatedly baked in ambient air at increasing temperatures from 100 °C to 300 °C in steps of 25 °C with a TA in-between each bake. Electrical measurements were performed after each bake/TA (meas. 3 to 20). All electrical measurements were carried out in N_2 after cooling the devices down to room temperature. An anneal at 300 °C in N_2 was furthermore performed after the final bake in air at 300 °C, however the increased temperature of the TA could not reverse the degeneration of the graphene FoM (meas. 21). Fig. 5.4 shows the mobilities and doping levels for two devices (D6 and D7) at measurement 1 to 21.

The mobility and doping for the two devices were recovered after the bakes in air until

200 °C by a TA. Raman spectra were obtained from these devices before any processing and after baking up to 300 °C in air (supplementary Fig. S.6 of [46]). A shift in the G peak position from $1585\,\mathrm{cm}^{-1}\pm2\,\mathrm{cm}^{-1}$ to $1598\,\mathrm{cm}^{-1}\pm3\,\mathrm{cm}^{-1}$ and a reduction from ~ 3 to ~ 1 in the 2D to G intensity ratio was observed; which corresponds to a considerable increase of the doping level according to [109]. A similar result was observed previously using Raman spectroscopy [108]. The observed irreversible doping can be due to an increased reactivity with O_2 [108] and/or induced carbon contamination [93] as a result of the high baking temperatures, as previously pointed out.

These results indicate that the graphene interact with air in an irreversible and undesirable manner when baked at a temperature above 200 °C in air, and such temperatures should therefore be avoided in graphene fabrication processes.

5.1.3 Influence of SF_6 Etch

We found that when shaping stacks of hBN-encapsulated graphene the SF_6 etch did not etch the graphene. It is worth noticing that our etch only contains SF_6 gas, whereas often a combination of a fluorine gas and oxygen or argon is used [21, 23, 73]. Graphene stencil devices were used to test the influence of the SF_6 etch with both electrical measurements and Raman spectroscopy.

It is known from literature that graphene on SiO_2 becomes fluorinated when exposed to a SF_6 plasma [84, 85]. In fluorinated graphene or fluorographene the hybridisation of some of the carbon atoms is changed from sp^2 to sp^3. The sp^3 hybridised carbon atom then bonds to one fluorine atom with a bond perpendicular to the graphene plane. Monolayer graphene is more affected by the SF_6 plasma than bi- and trilayer graphene, which is attributed to monolayer graphene being more corrugated compared to thicker layers of graphene. Furthermore, the fluorination has been demonstrated reversible by vacuum annealing at 970 K [84].

Stencil devices of mono- and bilayer graphene were used for this study. Graphene was exfoliated with blue tape on 107 nm SiO_2 and contacted with pure gold stencil contacts as described in Sec. 4.4 and fabrication scheme in Box 1. The stencil devices were first characterised electrically and with Raman spectroscopy (meas. 1), then thermally annealed at 250 °C and characterised once more (meas. 2). All electrical measurements and thermal anneals are carried out in a nitrogen atmosphere. The Raman spectra are obtained under ambient conditions, hence, the doping of the graphene will change in-between the electrical measurement and the Raman spectrum, as described in Sec. 5.1.1. The stencil devices were after the initial characterisation exposed to two SF_6 etch steps, first for 30 s and then for 60 s. Both etch steps were followed by electrical measurements and Raman spectroscopy, before and after a temperature anneal (meas. 3-6). FoM for both electrical measurements and Raman spectra are plotted in Fig. 5.5. The peaks of the Raman spectra are fitted with a Lorentzian function to obtain the FWHM.

Illustration of the two-terminal stencil devices and scheme of the field-effect measurements configuration are seen in Fig. 5.5a. The mobility is obtained by fitting Eq. (2.14) to the two-terminal field-effect measurements as in [46]. Plotted in Fig. 5.5b is the hole mobilities as the devices tend to become positive doped preventing measurements of the electron mobilities. To obtain the electron mobility of heavily positive doped devices, field-effect measurements at too high voltages would be needed, which lead to an irreversible break down and leakage through the gate dielectric. The mobilities are, to ease the comparison of the mono- and bilayer graphene devices, plotted in percent of the mobility obtained after the first temperature anneal (meas. 2).

Both the monolayer and bilayer devices become more p-doped as they are etched, the doping is to some degree reversed by thermal annealing, see Fig. 5.5c. The doping of the monolayer device increases to a value too high to reach with the back-gate, an estimation of the doping is therefore plotted outside the graph, for these two measurements (meas. 3 and 5), to illustrate

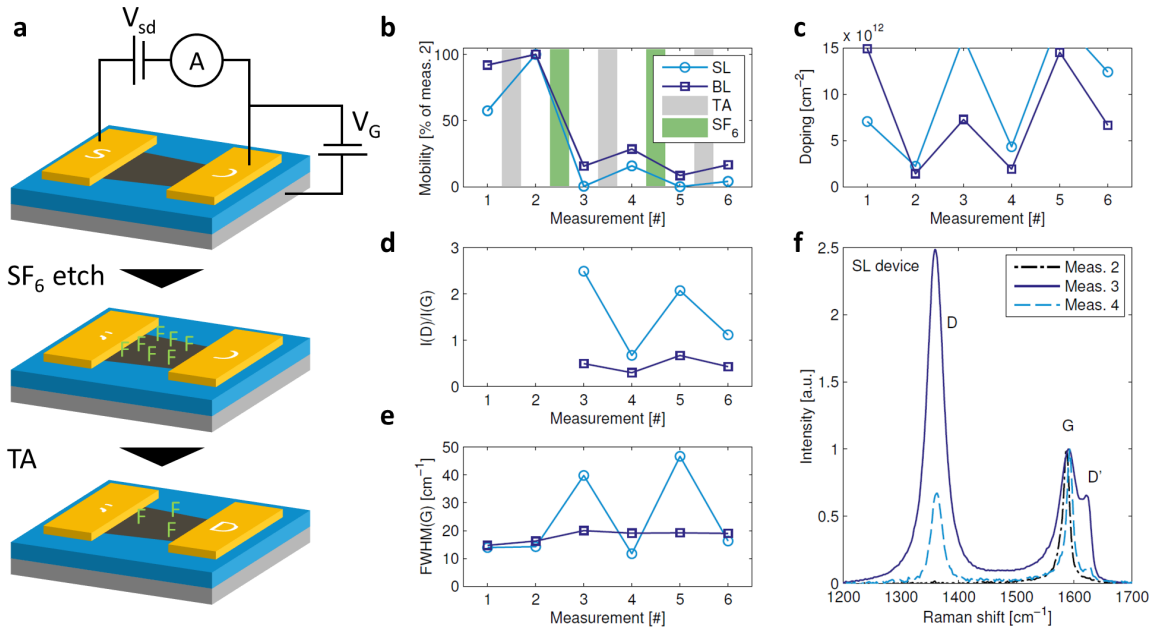


Figure 5.5: *(**a**) Sketch of the stencil device and the influence of the etch and temperature anneal. FoM from electrical measurements and Raman spectra obtained at the following six stages: (1) Initial measurement on as-fabricated stencil device. (2) After 30 minute temperature anneal at 250 °C. (3) After 1st SF_6 etch (30 s). (4) After TA. (3) After 2nd SF_6 etch (60 s). (4) After TA. The evolution of (**b**) mobility and (**c**) doping of the monolayer (ML) and bilayer (BL) device throughout the six stages. (**d**) I(D)/I(G) ratio and (**e**) FWHM(G) from the Raman spectra. (**f**) Raman spectra of the D, G and D' peaks of the monolayer device at measurement 2 – 4.*

the evolution of the doping.

The monolayer device is generally more affected by the SF_6 etch, and has a poorer recovery by the TA compared to the bilayer device. The mobilities at measurement 6 (after 30 s+60 s etch and TA) are reduced to 4 % and 17 % for the mono and bilayer, respectively.

The Raman data is plotted in Fig. 5.5d-f. The I(D)/I(G) ratio and the FWHM(G) for the monolayer device are clearly increased after the two SF_6 etches (meas. 3 and 5 in in Fig. 5.5d and e), which indicates an increase in the defect density, which to some extent is recovered after the TA (meas. 4 and 6). A similar trend is observed for the bilayer device, but less pronounced. Furthermore, the defect related peaks D' and D+D' appear after the etch steps. The intensity of these peaks is reduced but not eliminated after the thermal anneals. The Raman spectra of the D, G and D' peaks are seen Fig. 5.5f. No D and D' peaks are observed in the spectrum after the first temperature anneal (meas. 2), but the D' peak clearly appears in meas. 3, after the 30 s SF_6 etch and are reduced after the subsequent temperature anneal (meas. 4).

It is clear from the electrical measurements and the Raman signal that the graphene on SiO_2 is damaged from the SF_6 etch. In the stacks the graphene is assumed to be less damaged, both because the graphene is exposed to a shorter SF_6 etch than what was tested here, but also because the graphene will be less corrugated on a hBN flake compared to the SiO_2 surface [47] reducing the fluorination of the graphene [84].

The fact that the graphene is not etched by the SF_6 etch is important as it enables fabrication of more advanced structures. A monolayer of graphene can be used as a hard mask determining whether only the top-hBN or both the top- and bottom-hBN are etched in a hBN/graphene/hBN heterostructure. The use of graphene as a hard mask enables the 1D

corner contacts presented in Sec. 4.4.5. These contacts are critical for devices with graphite back-gated, where the etch has to be stopped at the graphene layer so the metal leads will not be shorted with the underlying graphite. This design is outlined in Sec. 5.3.

5.1.4 Summary

The use of stencil lithography combined with a systematic approach makes it possible to distinguish the impact of different processing steps on the electrical properties of graphene.

The evolution of hysteresis, doping and mobility of pristine contacted graphene through a sequence of PMMA processing steps was shown. The initial hysteresis of the pristine graphene was nearly eliminated by temperature annealing at 250 °C in N_2, and re-appeared in a reduced form upon exposure to air. A large initial variability of both the doping levels and hole carrier mobilities of the pristine graphene were observed and attributed to differences in the initial conformation to the SiO_2 substrate and particle contamination of the graphene. The dispersion of these values among the different devices is decreased during the PMMA processing steps. The devices were p-doped after the sequence of steps, and the data supports the notion that this p-doping is due to corrugation of the graphene rather than the actual PMMA residues on the graphene surface. The presumably uncorrugated graphene devices are subject to a mobility decrease during annealing processes in contrast to the normal case of graphene partly or fully conforming to the substrate even before the first measurement is carried out. Furthermore, the electrical properties of devices baked in air at temperatures below 200 °C were shown recoverable by temperature annealing. The observations here thus reconcile published Raman data of pristine graphene and electrical measurement on conventional devices. Finally, the influence of etching graphene, with the SF_6 etch used for etching of hBN and TMDs, was investigated. Graphene can withstand the SF_6 etch, however it can not retain its original electrical properties with the tested annealing.

This work shows that the stencil device approach is a cheap, fast, simple, yet powerful platform for the systematic optimisation and fault-finding invariably needed for fundamental research as well as commercialisation of graphene-based electronic devices.

Several of the issues related to substrate, processing and contamination can be entirely avoided with the development of the van der Waals assembly of hBN-encapsulated graphene devices. Fabrication and characterisation of devices with hBN-encapsulated graphene are presented in the next section.

5.2 hBN-Encapsulated Graphene

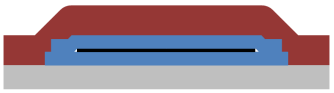
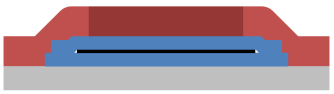
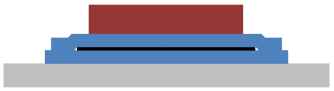
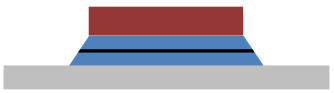
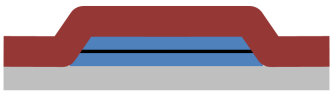
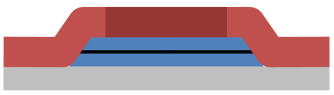
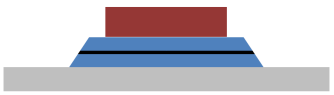
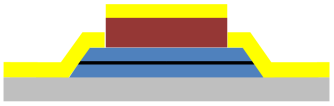
The work presented in this section has been equally distribute between Bjerke Sørensen Jessen, Filippo Pizzocchero and myself.

This section contains data from hBN-encapsulated graphene devices made by the vdW assembly method. Data from a large batch of hBN-encapsulated mono-, bi- and trilayer graphene and from devices of high density nano-patterned graphene are presented.

The advantages of hBN-encapsulation include; the hBN flakes are flat, have no dangling bonds, and the phonon modes in hBN do not limit the mobility as for SiO_2, see more details in Sec. 2.2.5. Moreover, the vdW assembly method yields atomically clean interphases between hBN and graphene flakes, and thereby reduces scattering of the charge carriers and doping of the graphene. Furthermore, the full encapsulation shields the graphene from polymer and solvent involved in the device fabrication. All in all, it is both an ideal substrate for graphene and an ideal passivation layer against the environment.

Box 2: Standard hBN/G/hBN heterostructures

Fabrication steps from an assembled hBN/graphene/hBN heterostructure to a shaped and contacted device.

Illustration	Step	Parameters
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Pos-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Etch	PMMA Descum 5 s O_2/Ar Top-hBN 20 s SF_6 Graphene 20 s O_2/Ar Bottom-hBN 20 s SF_6
	Resist strip	Rinsed in acetone + IPA + N_2 blow-dry
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Pos-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 600-1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Metallisation	5/50 nm of Cr/Au or 2/15/30 nm of Cr/Pd/Au
	Metal lift off	Chip is immersed in heated acetone for approximately 20 minutes. The process may be helped by adding turbulence with a pipette

5.2.1 Mono-, Bi- and Trilayer Graphene

The following section is based on the results published in [20] (F. Pizzocchero, L. Gammelgaard, B. S. Jessen, *et al.*). A set of 22 hBN-encapsulated graphene devices was batch-fabricated with the hot pick-up method described in Sec. 4.2. A total of 16 monolayer devices were fabricated, ten of a Hall bar geometry and six of a square geometry. The remaining six devices are Hall bars with bi- and trilayer graphene, three of each.

The hot pick-up method eliminates blisters between the layers even when assembling in an ambient atmosphere. Furthermore, the elevated temperature of 110 °C in the hot pick-up method enables a close to 100 % pick-up yield of graphene, even for monolayer graphene exfoliated on a plasma treated substrate. Graphene is generally more difficult to pick-up from a plasma treated substrate, but mechanical exfoliation on plasma treated substrates are favourable as larger flakes are obtained [76]. The Raman spectra (2D/G) recovered after the graphene had been picked up, suggesting that the graphene quality is not affected permanently by having been in contact with the plasma treated surface [20].

After assembly, the vdW heterostructures are first etched into the desired shape and then contacted with 1D edge contacts. The shape and contacts are defined by electron beam lithography. Fabrication steps from a vdW assembled stack to a shaped and contacted device are outlined in fabrication Box 2 together with side-view illustrations and parameters of the individual steps.

A false coloured SEM micrograph of a Hall bar shaped device is shown in Fig. 5.6a. Metal leads of either Cr/Au or Cr/Pd/Au are used for the 1D contact to the encapsulated graphene, as illustrated with the inset in Fig. 5.6b. The 22 devices were electrically characterised with four-terminal field-effect measurements at the probe station, at which the measurements are carried out at room temperature in an ambient atmosphere. Four-terminal resistivity versus gate induced charge carrier density are plotted in Fig. 5.6c for a representative mono-, bi- and trilayer device, and their corresponding mobilities are plotted in Fig. 5.6b.

While the monolayer devices show a maximum in mobility at a charge carrier density close to the charge neutrality point, the mobilities of the bi- and trilayer devices increases with charge carriers. Bi- and trilayer graphene dose not have a linear dispersion relation as monolayer graphene, which results in a difference in the short and long range scattering effects on the charge carrier mobilities, for details see Sec. 2.2.

An overview of the room temperature charge carrier mobilities of the 22 devices is shown in Fig. 5.7a. The Hall bar shaped devices have several contacts along the channel, as the device shown in Fig. 5.6a. Measurements are performed in various combinations, and multiple mobilities are therefore obtained for the Hall bar shaped devices. The van der Pauw (vdP) technique is used on the square devices. Eq. (2.18) is applied to find the sheet resistivity and thereby one value for the hole mobility and one for the electron mobility of the device. The square devices have side lengths of 3 µm, 5 µm and 10 µm, and the contacts used for the vdP measurements are located in the corners of the squares.

Field-effect mobilities up to 117,000 cm^2/Vs were measured for the monolayer graphene devices, and the bi- and trilayer devices yield electron mobilities up to 37,000 cm^2/Vs and 23,000 cm^2/Vs, respectively. The mobility values of the bi- and trilayer devices are comparable with the highest values reported at room temperature for such devices [24, 110, 111]. The monolayer graphene devices generally have a higher hole mobility compared to the electron mobility. This picture is reversed for the bi- and trilayer devices, where the electron mobility, for all but one measurement, is higher than the hole mobility, see plot of Fig. 5.7a and mean values of the mobilities in Table 5.1. These trends are consistent with published observations for mono-, bi- and trilayer graphene devices on a SiO_2 substrate [42].

The mean free path, λ_{mfp}, of the ten monolayer Hall bar and six square devices are in Fig. 5.7b-c plotted against the critical dimension, which is here understood as the smallest distance

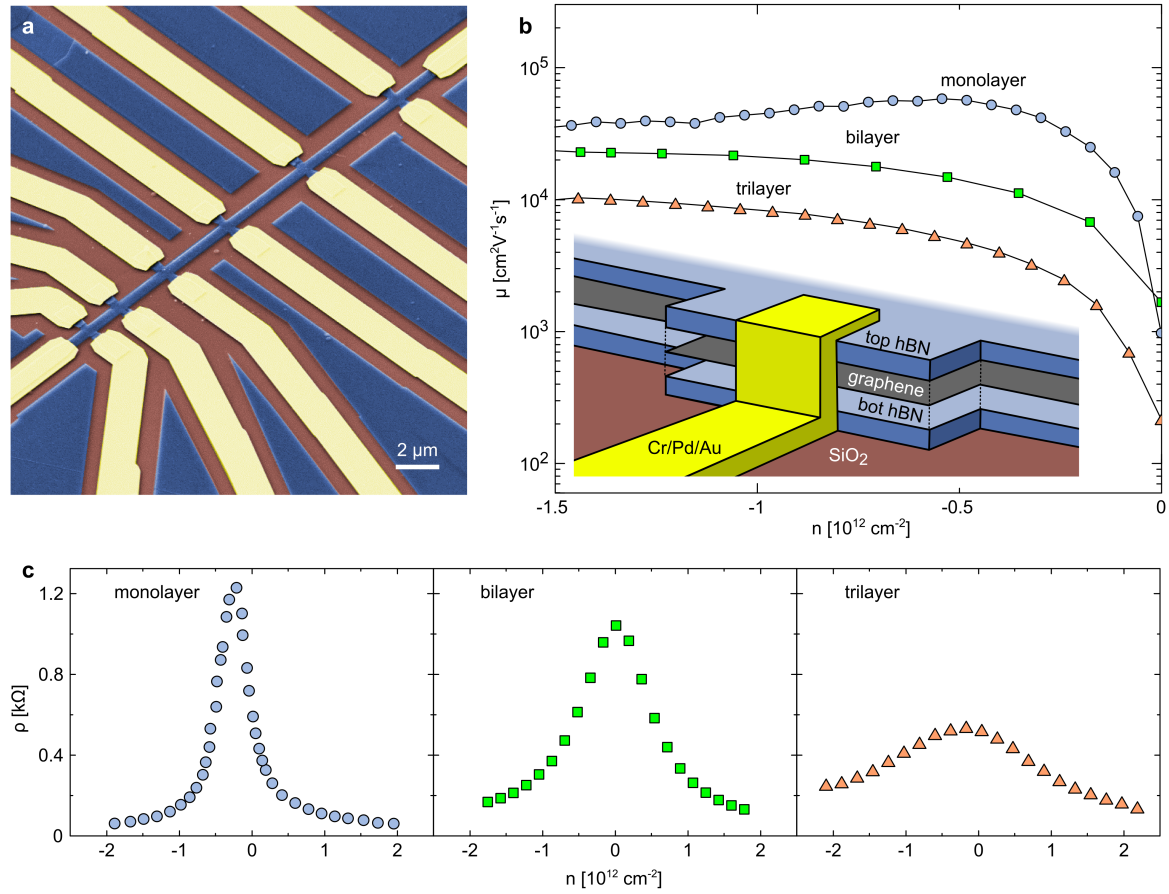


Figure 5.6: *(**a**) False colour scanning electron micrograph of encapsulated graphene device. Blue regions are unetched hBN and hBN-encapsulated graphene, brown are exposed SiO_2, and yellow regions are metal contacts. (**b**) Room temperature field-effect mobility measurements for representative monolayer (# 4), bilayer (# 11) and trilayer (# 14) Hall bar devices. A monolayer device displaying diffusive transport is shown. Blue/◯, green/□ and orange/△ indicate mono-, bi- and trilayer results respectively. Inset shows exploded schematic of contact region. (**c**) Resistivity vs. gate induced carrier density for mono-, bi- and trilayer graphene Hall bar devices. Colour scheme as in (**b**). Published in [20].*

Table 5.1: *Mean and standard deviation of the hole and electron field-effect mobility for the four device types. For monolayer $\mu_h > \mu_e$ and for bi- and trilayer $\mu_h < \mu_e$.*

Graphene thickness	Geometry	μ_h [cm^2/Vs]	μ_e [cm^2/Vs]
Monolayer (10 dev)	Hall	$44{,}500 \pm 26{,}000$	$42{,}000 \pm 24{,}000$
Monolayer (6 dev)	Square	$38{,}000 \pm 15{,}000$	$36{,}000 \pm 12{,}000$
Bilayer (3 dev)	Hall	$17{,}000 \pm 4{,}000$	$24{,}500 \pm 7{,}000$
Trilayer (3 dev)	Hall	$13{,}000 \pm 3{,}000$	$19{,}000 \pm 2{,}500$

between opposing boundaries except inside the leads. The critical dimension is for the Hall bar devices defined as the width of the channel, and for the square devices the side length. Eq. (2.5) is applied to calculate the mean free paths. Seven of the ten monolayer Hall devices show $\lambda_{mfp} \geq w/2$ (55 % of the measurements). Moreover, 19 % of the measurements on monolayer

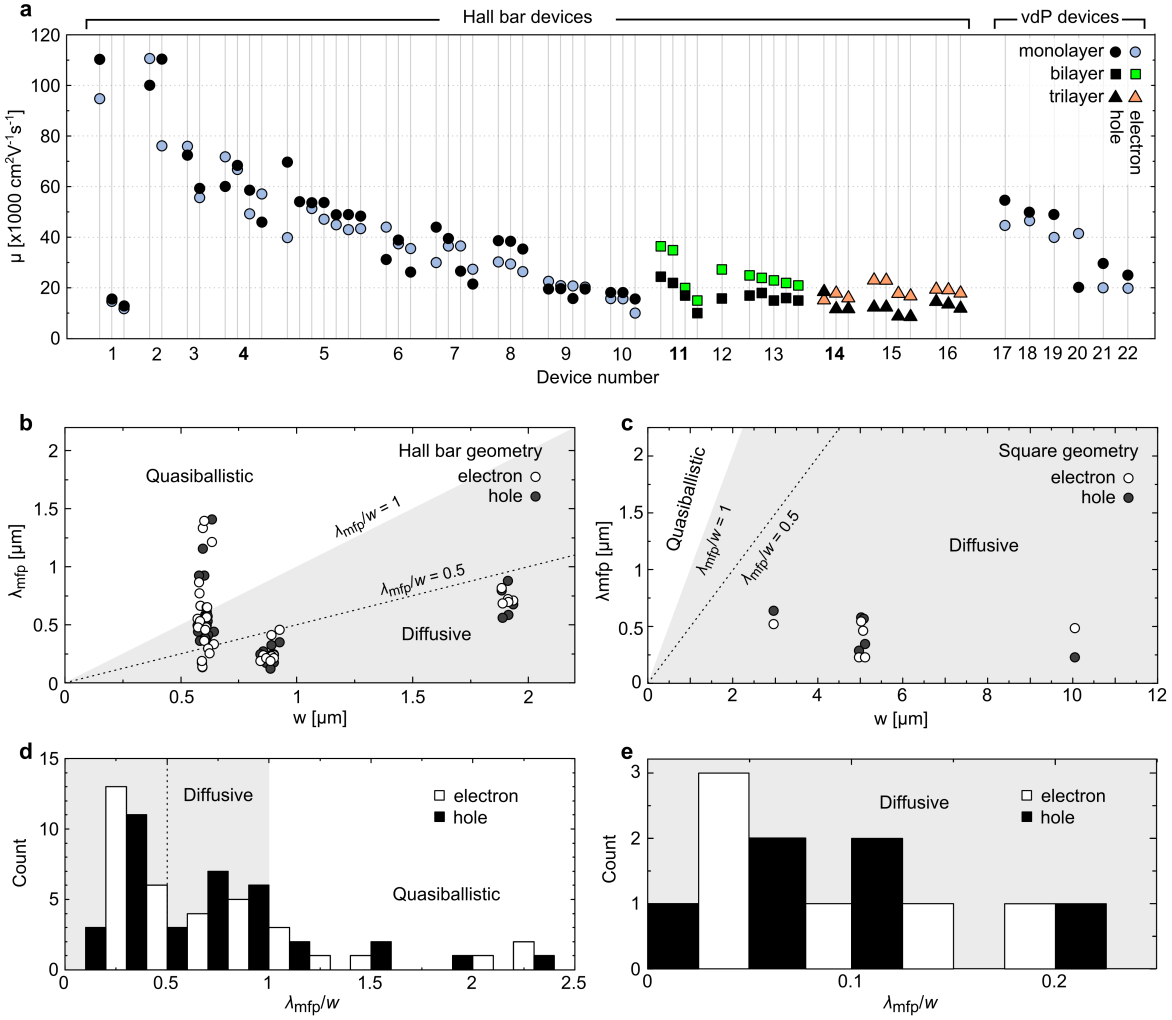


Figure 5.7: *Mobility and mean free path statistics.* (**a**) *Room temperature field-effect carrier mobility plot for all the devices (Hall bar and square) in this study.* (**b**) *Plot of electron and hole mobility for all monolayer Hall bar devices. Quasiballistic ($L > \lambda_{mfp} > w$) and diffusive ($w > \lambda_{mfp}$) regimes are indicated by the gray region.* (**c**) *Plot of electron and hole mobility for all square monolayer devices. Quasiballistic and diffusive regimes are indicated by the gray region. The average mean free path is 450 nm±170 nm and 420 nm±140 nm for holes and electrons respectively.* (**d**) *Histogram of monolayer electron and hole mobilities for all Hall bar devices.* (**e**) *Histogram of monolayer electron and hole mobilities for all square devices. Published in [20].*

Hall devices are quasiballistic, as the mean free path exceeds the critical dimension while being smaller than the device length, $L > \lambda_{mfp} > w$ [30, 112, 113]. The transport is assumed limited by boundary scattering since the calculated mean free paths, in particularly for the narrow devices, are comparable to or larger than the device width [114]. Histograms of the mean free path relative to the device width are seen in Fig. 5.7d for the Hall bar shaped devices and in Fig. 5.7e for the square devices. The average mean free path at room temperature of the hole and electron carriers in the vdP measurements of the square devices is 450 nm ± 170 nm and 420 nm ± 140 nm, respectively.

The vdW assembly method of [20] (described in details in Sec. 4.2) is a facile and robust technique for batch assembly of vdW heterostructures. It has here been employed to fabricate a large batch of mono-, bi- and trilayer graphene devices. These devices have been electrically

characterised and quasiballistic behaviour has been observed at room temperature. Furthermore, electron mobilities consistent with the highest reported for bi- and trilayer devices have been measured.

5.3 Graphene Antidot Lattice

The work presented in this section has been equally distribute between Bjarke Sørensen Jessen and myself.

One of the motivations to make graphene antidot lattices (GAL) is to turn the semimetal graphene into a semiconductor by opening a band gap. A periodic perturbation of the graphene is theoretically predicted to open a gap [115]. The dimensions of the structure determine the size of the gap. The GAL structures are characterised by the period of the holes (centre to centre distance), the diameter of the holes, and the neck-width in-between the holes, see upper left part of Fig. 5.8. Small periods are of interest to realise gaps of reasonable sizes, as the energy gap E_g of a GAL structure can be approximated by the following equation [115]

$$E_g = 25\,\mathrm{eV}\frac{\sqrt{N_{removed}}}{N_{total}}\ , \tag{5.1}$$

where N_{total} is the total number of atoms in the GAL unit cell and $N_{removed}$ is the number of removed carbon atoms within the unit cell. This rough approximation do not take edge roughness of the holes, misalignment of the holes or other structural defects into consideration, which realistically will be present in a fabricated devices. Nevertheless, it will be used here to give an idea of the possible size of a gap, as the structural defects are expected to have detrimental effects of the band gap [116].

Nevertheless, it will be used here to give an idea of possible gap size. Structural defects are expected with realistic lithographic processes, unfortunately such defects have theoretically shown to detrimental effects of the band gap [116].

Gaps sizes calculated by Eq. (5.1) for triangular GAL structures with periods and hole diameters up to 150 nm are plotted as a contour map in Fig. 5.8, where lines indicated various gap sizes. It is clear that small periods and large holes are needed to create energy gaps sufficiently larger than the thermal energy at room temperature. GAL structures with periods below 50 nm have until now mainly been realised by patterning with bottom-up approaches such as block-co-polymers, BCP, lithography. Patterning with BCP has the great advantage of being scalable, however, it is also difficult to control the precise arrangement of the structures. Here devices with structures of 35 nm and 45 nm periods are fabricated with EBL. Such small structures are normally not fabricated with EBL. See the published work plotted in the contour plot of Fig. 5.8.

Theoretical work has demonstrated that a few rows of holes in graphene should yield a band gap similar to that of a fully nano-patterned device [129]. This is promising as nano-patterning has shown to diminish the apparent mobility of the graphene radically. The smaller GAL area has been tested experimentally [127], in the hope that it would open a gap and maintain a high mobility. Here graphene devices on SiO_2 were patterned with one row, five rows and a mesh (42 rows) of antidots with a period of 55 nm. While the one row and five rows area show a smaller reduction in mobility compared to the mesh, cleaner devices and more studies are need to see whether this would be a solution to open a gap in graphene while retaining the favourable high mobility.

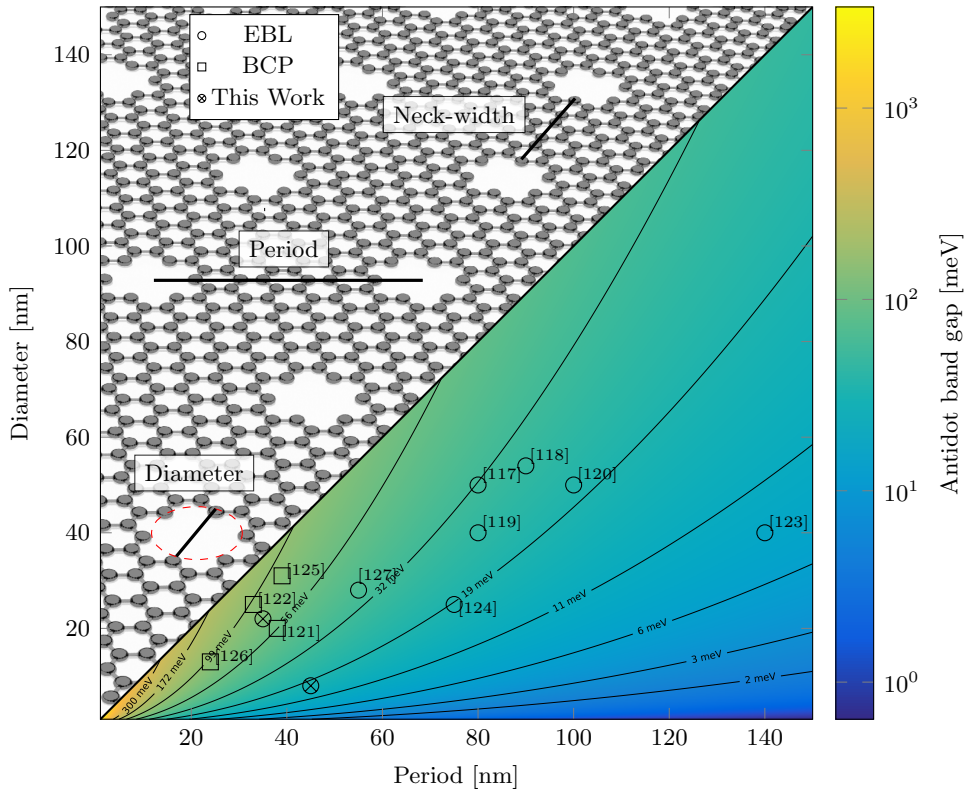


Figure 5.8: *Energy gap of graphene antidot lattice calculated with Eq. (5.1) plotted together with published work of GAL structures fabricated by E-beam and BCP lithography. Small periods with large hole diameters are needed to obtain gaps of reasonable sizes. Small dimensions are mainly obtained by BCP lithography, and the devices of this work. GAL background image is adapted from [128].*

The outcome of vdW heterostructure of graphene is above all expectations and GAL structures into hBN-encapsulated graphene have recently been reported to yield ballistic transport [124, 130]. The transport in the GAL structures is considered ballistic when the mean free path of the charge carriers is larger than the critical dimension of the GAL structure. The critical dimension for the GAL is here defined as the period of the GAL.

Constructing GAL in hBN-encapsulated graphene is of interest as the hBN-encapsulation both produces high quality devices and protects the graphene during processing and etching. Optimisation of the high density nano-patterning, fabrication of hBN-encapsulated GAL devices and electrical measurements of these devices have been carried out together with fellow Ph.D. student Bjarke Sørensen Jessen, and will be outlined below.

5.3.1 Nano-Patterning

Decreasing the dimensions of the GAL structures is challenging, and dose testing and process optimisation were therefore first done on plain silicon wafers and then on hBN flakes before patterning of real devices. The initial dose testing on silicon wafers was used both to find the suitable parameter spectrum for the EBL, and to test various process parameters, such as; polymer thickness, development time and solvent, etching with and without a descum etc. The final optimisation was done on hBN flakes before determining the E-beam doses and parameters to be used for structuring of devices of hBN-encapsulated graphene. Dose testing and etch test in silicon and hBN have been carried out for both square and triangular lattices, however, only triangular lattices have been made in devices so far.

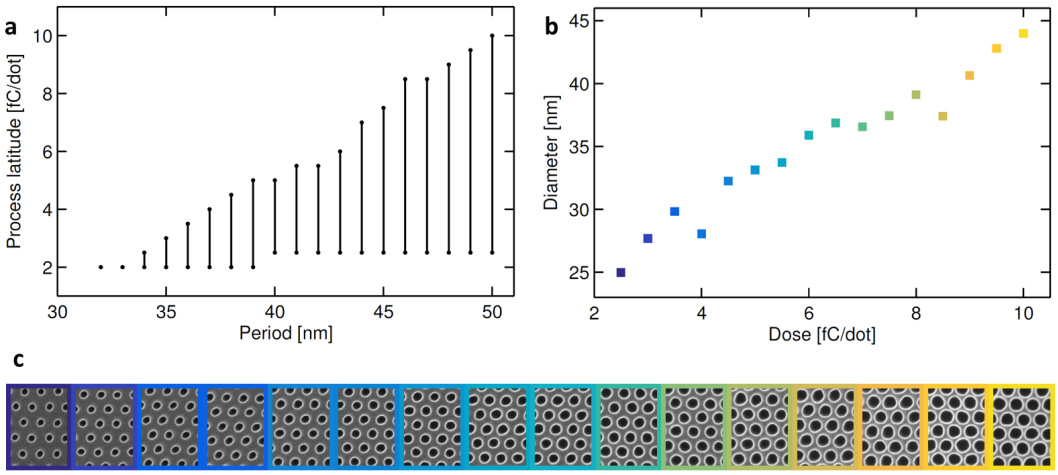


Figure 5.9: *(**a**) Process latitude of the E-beam dose as a function of the period of a triangular antidot lattice etched into silicon. For doses to be in the process latitude all holes have to be present and no holes may be merged in the 2 µm by 2 µm area of the antidot lattices. (**b**) Diameter variation with increasing dose for the 50 nm period antidot lattice. (**c**) Sections of SEM micrographs of the 50 nm period images used for the plot in (**b**), the images are colour framed to match the plot.*

In the initial testing two approaches, normal and single-shot exposures, were explored for the nano-patterning. In normal exposures a hole/antidot is defined to have a certain area and the beam is then moved across this area exposing the area with multiple shots. For single-shot exposure each hole is made by only one shot where the beam is kept at a fixed position [131], hence the hole is designed as a point, not an area. The single-shot exposures were observed to yield the best initial results and were therefore further optimised for nano-patterning in both silicon and hBN. The unit of E-beam doses is normally given as Coulomb per area, but is here converted to Coulomb per dot, as this is more informative for the single shot exposures. The E-beam exposures of nano-patterns are performed in the JEOL JBX-9500FSZ 100 keV E-beam system at DTU Danchip with low current of 0.2 nA, as the currents below 6 nA generally gives smaller and more circular holes [131].

PMMA is an excellent high-resolution electron-beam resist, and a thin layer of ~ 50 nm PMMA has been used for the nano-patterning. Fabrication of dense nano-patterns requires a low aspect ratio between then dimensions of the antidot lattice and the thickness of the PMMA. However, the PMMA was not spun thinner as it both has to be uniform and must withstand etching when the pattern is transferred from the PMMA into the underlying substrate.

The etch used for silicon was optimised to etch similar to the hBN etch to ease the transfer of the process from silicon to hBN flakes. Overview of selected results from the test on silicon is seen in Fig. 5.9. For a dose to be in the process latitude plotted in Fig. 5.9a, all holes have to be present and no holes should be merged in the whole dose test area of 2 µm by 2 µm. The process latitude gets narrower for the small periods. Antidot lattices of periods down to 25 nm have been constructed, however such structures have both missing and merged holes for the same doses and further optimisations would be needed to realise such small structures without defects. A large range of doses are within the process latitude of the structures with larger periods. The dose can for these structures be used to modify the hole diameter, contrary to normal EBL exposures, where the diameter of a hole would be changed by changing the dimensions of the design written by the E-beam. The plot of Fig. 5.9b shows a linear increment of the hole diameter with increasing dose of the large process latitude of the 50 nm period. The diameter is calculated through image analysis of SEM micrographs of the antidot lattice,

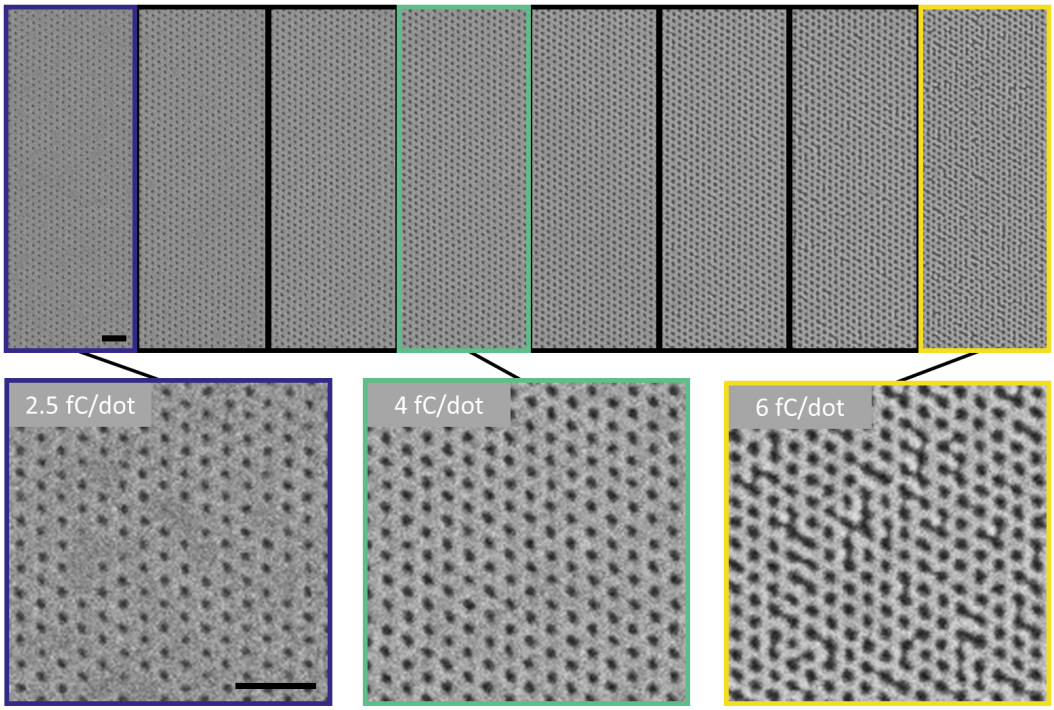


Figure 5.10: *SEM micrographs of 30 nm period antidot lattices etched into a hBN flake. (Top) SEM micrographs of antidot lattices exposed with doses from 2.5 fC/dot to 6 fC/dot in steps of 0.5 fC/dot. Holes are missing for the low doses where the structure is under-exposed (bottom left), and for the high doses holes starts to merge and the structure is over-exposed (bottom right). At a dose of 4 fC/dot (bottom center) all holes are present and no holes are merged in the 2 μm by 2 μm area of the dose test. The scale bars are 100 nm.*

segment of the SEM micrographs are lined up in Fig. 5.9c.

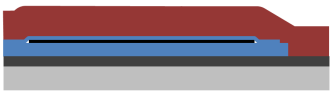
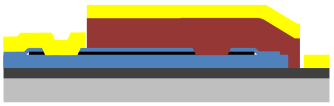
After optimisation on silicon wafers, single-shot dose tests and optimisation were carried out on hBN flakes exfoliated onto a substrate of Si/SiO_2. SEM micrographs of an antidot lattice with a period of 30 nm in a hBN flake are shown in Fig. 5.10. The process latitude of the 30 nm period is small as for the structuring in silicon wafers. A too low a dose clearly leads to an under-exposed structure with missing holes while too high a dose leads to over-exposure and merged holes. A dose of 4 fC/dot suits the structure, and shows the dense nano-pattern transferred into the hBN flake without missing or merged holes, see Fig. 5.10.

5.3.2 Device Fabrication

Devices of hBN-encapsulated graphene were finally nano-patterned to form a GAL structure in the hBN protected graphene. The pattern transfer through the hBN into the graphene has some challenging aspects. In particular, the SF_6 etch used for etching hBN is not vertical but has a $\sim 54\,^\circ$ angle leading to a cone-like structure being etched into the hBN when etching a hole. The top-hBN of the vdW hBN/graphene/hBN heterostructure will therefore have to be thin in order for the nano-pattern to reach the graphene. Assembly with thin top-hBN ($8\,\text{nm} \pm 4\,\text{nm}$) is more challenging compared to the normal stacks where top-hBN of thicknesses > 20 nm normally is used. First of all, the thin hBN flakes are often smaller and more rare when exfoliating. Secondly, vdW assembly at elevated temperatures is more difficult as the thin hBN tend to fold on the block of PDMS/PPC, for details see Sec. 4.2. However, the assembly at elevated temperatures is favourable in order to avoid interlayer contamination.

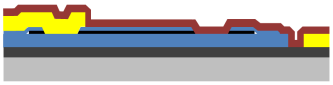
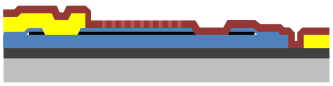
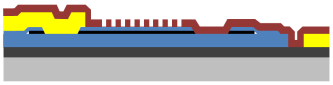
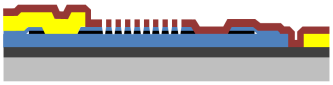
Box 3: Graphite back-gated hBN/G/hBN heterostructures

Fabrication steps to shape and contact a heterostructure of hBN-encapsulated graphene on a back-gate of graphite. A thin top-hBN is used for the heterostructure as the graphene will be nano-patterned through the top-hBN. The fabrication scheme for the nano-patterning is shown in Box 4.

Illustration	Step	Parameters
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Pos-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Etch	PMMA Descum 5 s O_2/Ar Top-hBN 20 s SF_6 Graphene 20 s O_2/Ar
	Resist strip	Rinsed in acetone + IPA + N_2 blow-dry
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Pos-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 600-1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Metallisation	5/50 nm of Cr/Au or 2/15/30 nm of Cr/Pd/Au
	Metal lift off	Chip is immersed in heated acetone for approximately 20 minutes

Box 4: Nano-patterning of hBN/G/hBN heterostructures

Fabrication steps to nano-pattern graphene in a heterostructure with a thin top-hBN.

Illustration	Step	Parameters
	Resist spin	Pre-bake: 10 min @ 180 °C 2 % PMMA in anisol: spin speed of 3500 rpm, acc. of 500 rpm for 1 min Pos-bake: 10 min @ 180 °C
	E-beam exposure	Single-shot exposure Current: 0.2 nA Dose: 3.5 fC/dot – 4.5 fC/dot
	Development	30 s IPA N_2 blow-dry
	Etch	Top-hBN 15 s SF_6 Graphene 15 s O_2/Ar
	Resist strip	Rinsed in acetone + IPA + N_2 blow-dry

Furthermore, an additional step of complexity was added to the fabrication as the stacks were made with a graphite back-gate. The graphite serves both as a flat substrate and moreover it screens long-range potentials in the graphene channel better as the hBN used as gate dielectric is thinner than the SiO_2 normally used [27, 41], for more details see Sec. 2.2.4.

The stacks with graphite back-gates have to be contacted without etching the bottom-hBN, and the one-dimension corner contacts, introduced in Sec. 4.4.5, are therefore made on these devices. The advantage of these contacts are that they are made without etching the bottom-hBN, making it possible to contact the graphene without the metal leads shorting with the graphite back-gate. The etch process for shaping of the device is therefore one step shorter than for a normal stack, and the ability of graphene to act as etch stop for the SF_6 etch is taken advantage of to stop the edge, see details of the etch in Sec. 4.4.3 and Sec. 5.1.3. The fabrication steps from assembled vdW heterostructure to contacted device are outlined in fabrication Box 3, with typical parameters for the steps and side-view illustrations.

The devices are electrically characterised at room temperature before nano-patterning the device channel, in this way the initial properties of the pristine device are known. The GAL structures in stacks are fabricated with single-shot exposures optimised in silicon and hBN flakes. Details of the nano-patterning of the contacted devices are seen in fabrication Box 4. The etching times of the hBN and graphene are reduced to 15 s each to spare the thin PMMA layer used for nano-patterning. However these etch times should be sufficient to etch ~ 100 nm hBN and ~ 3 nm of graphene while etching below 25 nm of the PMMA, (see Sec. 4.4.3).

Table 5.2: *Measured and estimated dimensions and band gaps of two GAL devices, one of a 35 nm period (device D1), and one with a 45 nm GAL periode (device D2).*

Parameter	**D1: 35 nm GAL**	**D2: 45 nm GAL**
Top-hBN thickness [nm]	6	12
Bottom-hBN thickness [nm]	30	30
Designed GAL period, p [nm]	35	45
Estimated graphene hole diameter, d [nm]	20-25	5-10
Estimated graphene neck-width [nm]	15-10	40-35
Estimated E_g [meV]	75 ± 8	15 ± 5

5.3.3 Results

Preliminary results from two devices, one of a 35 nm period and one of a 45 nm period of a triangular GAL structure, are here presented. All hBN flakes uses in the devices were inspected by AFM prior to the vdW assembly as the thickness of the top- and bottom-hBN flakes is important for etching and field-effect gating, respectively. The diameter of the holes etched into the graphene is estimates from the etch angle of $\sim 54\,^{\circ}$, the thickness of the top-hBN and the expected hole diameter at the top of the hBN. The GAL of a 35 nm period is made in a stack with a 6 nm thin top-hBN leading to an estimated graphene hole diameter (neck-width) of 20 nm to 25 nm (10 nm to 15 nm). The 45 nm GAL period is made in a stack with a thicker top-hBN of 12 nm and with the same dose as the one used for the 35 nm GAL. This leads to both smaller holes at the top of the hBN and in the graphene. A hole diameter (neck-width) of 5 nm to 10 nm (35 nm to 40 nm) is estimated of the graphene in the 45 nm GAL device. The diameters at the top of the hBN are estimated from SEM micrographs of test structures in hBN flakes fabricated in the same manner as the one in the devices. The band gaps of the two GAL devices estimated with Eq. (5.1) are in the order of $15\,\text{meV} \pm 5\,\text{meV}$ and $75\,\text{meV} \pm 8\,\text{meV}$ for the 45 nm and 35 nm GAL, respectively. Measured and estimated dimensions and band gaps of the two hBN-encapsulated GAL devices are listed in Table 5.2.

The 35 nm GAL device was measured at room temperature and in ambient conditions both prior to the nano-patterning (Fig. 5.11a) and after the GAL nano-patterning (Fig. 5.11b). The device architecture of the GAL nano-patterned device is illustrated in Fig. 5.11d-e.

The device was negatively doped prior to the nano-patterning $n_{CNP} = 1 \times 10^{12}\,\text{cm}^{-2}$, and shifted to a zero net doping after nano-patterning. Furthermore, hysteresis was initially close to zero, but an increase is observed after nano-patterning. The resistance increases radically after nano-patterning, which is expected both as a significant part of the channel is etched away, and as more edges are present on which scattering occurs. Moreover, the characteristics of the conductance changes from a square root dependence, $\sigma \propto \sqrt{n}$, to a more linear behaviour, $\sigma \propto n$, indicating that Coulomb scattering is dominating in the nano-patterned device, see Sec. 2.2 for more details on the scattering mechanisms. The apparent hole and electron mobilities of the nano-patterned graphene are reduced to 3.6 % and 2.7 % of the initial mobility, respectively. The mean free paths were 154 nm for holes at the initial measurements at room temperature, and are reduced to 7 nm after nano-patterning, the electrons show similar changes. The initial and after GAL mobilities and mean free paths are listed in Table 5.3.

Room temperature mobilities and mean free paths of device D2 before and after nano-patterning with a 45 nm period GAL structure are also listed in Table 5.3. The apparent hole and electron mobilities are reduced to 31 % and 41 % of the initial mobility after nano-patterning, respectively. The smaller reduction in the mobilities is attributed to the larger period and larger neck-width of the 45 nm structure, hence less of the graphene is etched

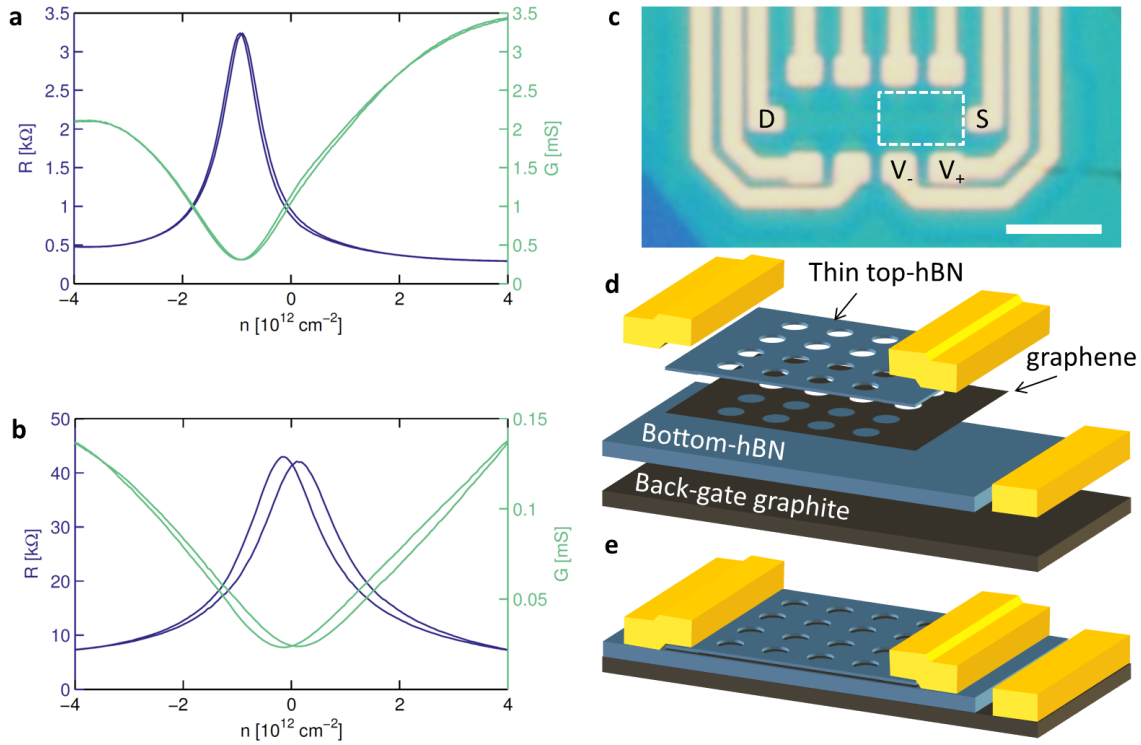


Figure 5.11: *Room temperature four-terminal resistance and conductance for hBN-encapsulated graphene prior to nano-patterning (**a**) and after nano-patterning of a 35 nm GAL structure (**b**). Device name D1. (**c**) Optical micrograph of the device. The probe configuration used for the measurements in (**a**) and (**b**) is marked. The LHS of the devices is kept pristine and RHS, the framed area, of the devices is nano-patterned. The device outline is difficult to distinguish as only the 6 nm thin top-hBN and graphene is etched. Scale bar is 4 µm, and the contrast has been enhanced. The dashed box indicates the area of GAL nano-patterning. (**d**-**e**) Illustration of the device structure with a graphite back-gate, a thin top-hBN and 1D corner contacts.*

away compared to the 35 nm device. The room temperature mean free path of the holes is prior to nano-patterning in the order of 220 nm. This is reduced to an apparent 55 nm after nano-patterning.

The 45 nm GAL device was also measured at temperatures from 2 K to 280 K in the TeslatronPT from Oxford instruments. The four-terminal measurements at the voltage probes V1 and V2 show a high asymmetry around the charge neutrality point at low temperatures,

Table 5.3: *Four-terminal measurements of the apparent hole and electron field-effect mobility, μ, and mean free paths, λ_{mfp}, for the GAL devices prior to (initial) and after nano-patterning (GAL). Measurements are performed at room temperature in ambient conditions. The mean free paths are at a induces carrier density of $\sim 10^{12}\,cm^{-2}$.*

Device	μ_h [cm^2/Vs]	μ_e [cm^2/Vs]	$\lambda_{mfp,h}$ [nm]	$\lambda_{mfp,e}$ [nm]
D1: initial	13,200	14,500	154	160
D1: 35 nm GAL	480	390	7	8
D2: initial	9,100	5,800	220	200
D2: 45 nm GAL	2,800	2,400	55	60

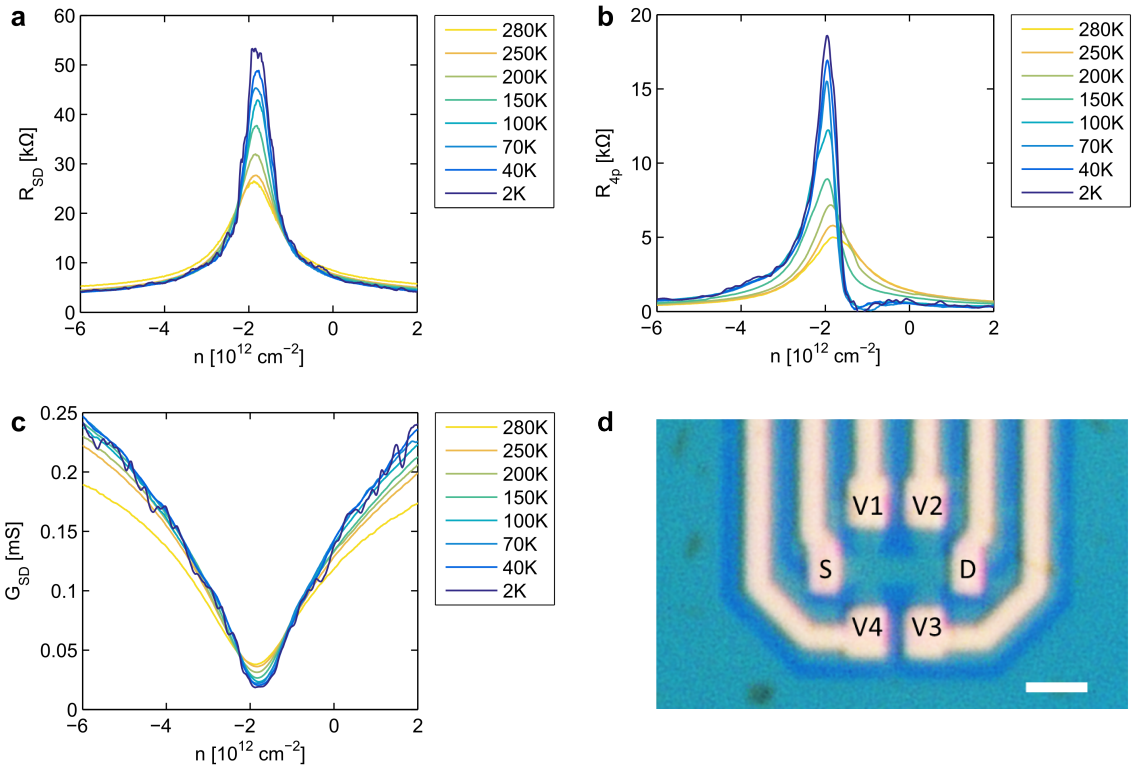


Figure 5.12: *Electrical data from the 45 nm hBN-encapsulated GAL device (device D2), at temperatures of 2 K to 280 K. (**a**) Two-terminal resistance measured between source to drain electrodes, and (**b**) four-terminal resistance measured at the probes V1 and V2. The resistance becomes highly asymmetric at low temperatures. (**c**) Source-drain conductance as function of the gate induced charge carriers. (**d**) Optical micrograph of the device, the entire device channel is patterned with a triangular GAL structure with a period of 45 mn. The scale bar is 2 µm and the contrasts have been enhanced.*

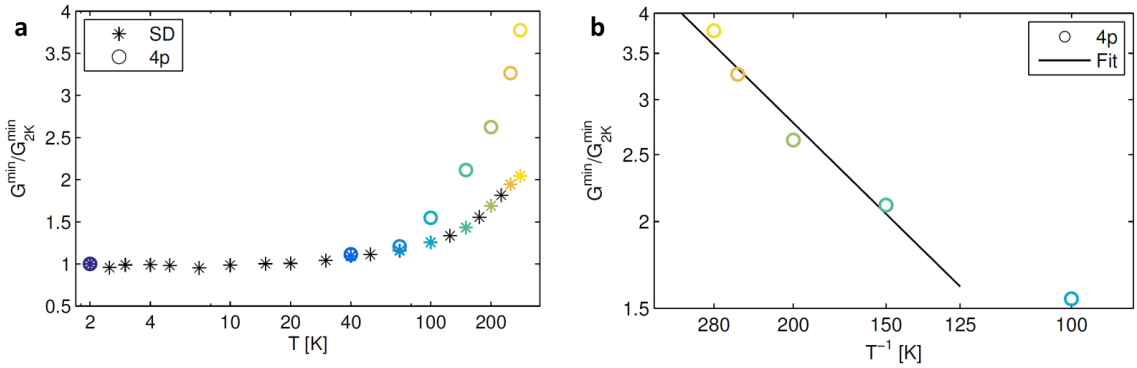


Figure 5.13: *(**a**) Temperature dependence of the minimum conductance at the CNP for both the two-terminal source to drain measurement and the four-terminal measurement between V1 and V2. (**b**) Arrhenius plot of the minimum conductance of the high temperatures from 100 K to 280 K.*

as shown in the plot of the two- and four-terminal resistance in Fig. 5.12a-b. The origin of the asymmetry of the four-terminal measurements is unknown. The conductance between the SD electrodes as function of induced charge carriers is plotted in Fig. 5.12c for varying temperatures. There is a clear temperature dependency on the minimum conductance, as seen

both in the gate sweeps of Fig. 5.12c, and plots is Fig. 5.13, where the minimum conductance normalised to its value at 2 K is plotted as a function of temperature. The interpretation of the temperature dependency of the two-terminal source-drain minimum conductance has to be conservative, as the source-drain measurements both include the resistance of the channel and the contacts. The temperature dependency of the contact resistance of 1D contacts to graphene in stacks has been shown to be very small [21] compared to top metal contacts to graphene on SiO_2. However, we have observed increasing contact resistance with decreasing temperature. The minimum conductance of the four-terminal measurements is also plotted in Fig. 5.13a, but these values may be effected by the observed asymmetry, nevertheless a clear temperature dependence is observed.

The temperature dependence at the minimum conductance may be a result of an energy gap. The current at the minimum conductance is dominated by thermally activated charge carriers and will follow a exponential dependence on temperature [27, 132, 133]

$$\sigma = \sigma_0 \exp\left(\frac{-E_g}{2k_B T}\right) \tag{5.2}$$

$$\ln(\sigma) = \ln(\sigma_0) - \frac{E_g}{2k_B}\frac{1}{T} \tag{5.3}$$

where E_g is the energy gap and k_B is Boltzmann's constant. The Arrhenius plot in Fig. 5.13b illustrates the temperature dependency of the minimum conductance at high temperatures with the fit of Eq. (5.3). A transport gap of 31.3 meV $\pm$ 9.1 meV is extracted from the relation of the six highest temperatures (280 K to 150 K) in the Arrhenius plot of the minimum four-terminal conductance, see Fig. 5.13b. However, this is an larger gap than expected and the Eq. (5.3) does not fit the Arrhenius plot of the four-terminal measurements well, another effect may therefore be involved.

Temperature dependencies of the minimum conductance of pristine graphene on SiO_2 is normally weak if any, which is attributed to a high residual carrier density, see Sec. 2.2.5 for details. The temperature dependency observed here may be a result of a low residual carrier density. An increase of a factor of three in the minimum conductance from low to room temperature has been measured for suspended graphene [31], and a factor of two has been observed between 4 K and 300 K for graphene on hBN [24]. We observed an increase of almost four in the minimum conductance from the four-terminal measurement from 2 K to 280 K.

Whether the temperature dependency is a result of a gap, a low residual charrier density, or a combination will remain unclear until devices of the architecture used for the 35 nm device has been measured. The GAL structure in the 35 nm device was only etched into half of the device, as indicated with a square in the optical micrograph in Fig. 5.11c. This design makes it possible to compare the region of pristine graphene and the GAL region simultaneously when cooling the sample down. This comparison in needed to separate the effect on the minimum conductance of a possible gap and a possible low residual carrier density.

These devices with GAL structures of periods down to 35 nm are to my knowledge the most dense structures defined via EBL in hBN-encapsulated graphene and in graphene in general. Furthermore, devices of smaller dimensions, possibly periods down to 25 nm, are within reach of the fabrication method. Some optimisation will be needed to obtainer perfect GAL structures of sub 30 nm periods, where all holes are present and none are merged, however the preliminary results are promising.

5.4 Summary

Graphene devices on a SiO_2 substrate and fully encapsulated in hBN have here been fabricated and electrically characterised. Graphene flakes on SiO_2 with contacts fabricated by stencil

lithography have been used as a tool for testing and optimising fabrication processes [46]. High quality vdW hetrostructure devices of mono-, bi- and trilayer graphene, fabricated with the hot pick-up method yield high mobility devices and mean free paths limited by the edges of the devices [20]. Finally, all 2D flake devices of high density nano-patterned hBN-encapsulated graphene with a graphite back-gate and 1D corner contacts have been fabricated. These are fabricated with the aim of opening a band gap in the semimetallic graphene.

6 Transition Metal Dichalcogenides

This chapter covers the results with transition metal dichalcogenides. First, the long-term stability and ageing of WSe_2 have been examined both with AFM inspections and electrically with stencil devices. Furthermore, devices of hBN-encapsulated and graphene contacted heterostructures of MoS_2 and $MoTe_2$ have been fabricated by vdW assembly and electrically characterised at temperatures down to 78 K.

Contents

6.1 Ageing and Protection of TMD Edges

In the following section it is shown that phase-imaging AFM of exfoliated multilayer WSe_2 flakes provides a direct identification of exposed and covered edges. The phase-imaging can therefore, together with the thickness variations measured by the topography AFM, be used to predict the arrangement of the layers in flakes. Steps with a low or no phase-contrast are strongly correlated with steps of long-term stability in ambient conditions, indicating that they are covered and effectively protected by above-lying WSe_2 layers. On the contrary, steps

with high phase-contrast are clearly degraded after long-term exposure to ambient conditions (up to six months). This assumed correlation between phase-contrast and the step order was confirmed by cross-sectional transmission electron microscopy (TEM).

6.1.1 Covered versus Exposed Steps

A large WSe_2 flake with regions of different layer thickness ranging from monolayer to nine layers was examined by tapping mode AFM over a six month period. The first AFM scans were performed shortly after exfoliation, and the following scans were performed after exposure to ambient conditions for two weeks, four and a half months and six months, respectively.

Topography and phase-contrast of the AFM of the pristine flake (initial) and topography of the aged flake are in Fig. 6.1 overlaid on an optical micrograph of the flake for comparison. The optical micrograph and topographic AFM both show a series of steps. From the optical contrast and thickness variations of the regions are identified as 9, 8, 5, 4, 3 and 2 layers, indicated with the notation 2L for two layers. The steps are of $6-7$ Å in height, as indicated in Fig. 6.1a, which matches well with the expected interlayer distance in WSe_2 of ~ 6.3 Å [134]. The phase-contrast AFM of the pristine flake shows that the steps either exhibit a large phase-shift (i.e. the 3L-4L step) or a negligible phase-shift (i.e. the 4L-5L step), see Fig. 6.1b. AFM topography imaging of the aged flake shows clear degradation at the boundary edge towards the SiO_2 substrate, as well as at the steps with high phase-contrast in the initial AFM scan. In contrast the steps with no phase-contrast in the initial AFM do not show any signs of degradation, see Fig. 6.1c.

WSe_2 is known to oxidise to tungsten oxide when heated up in ambient conditions [135] or

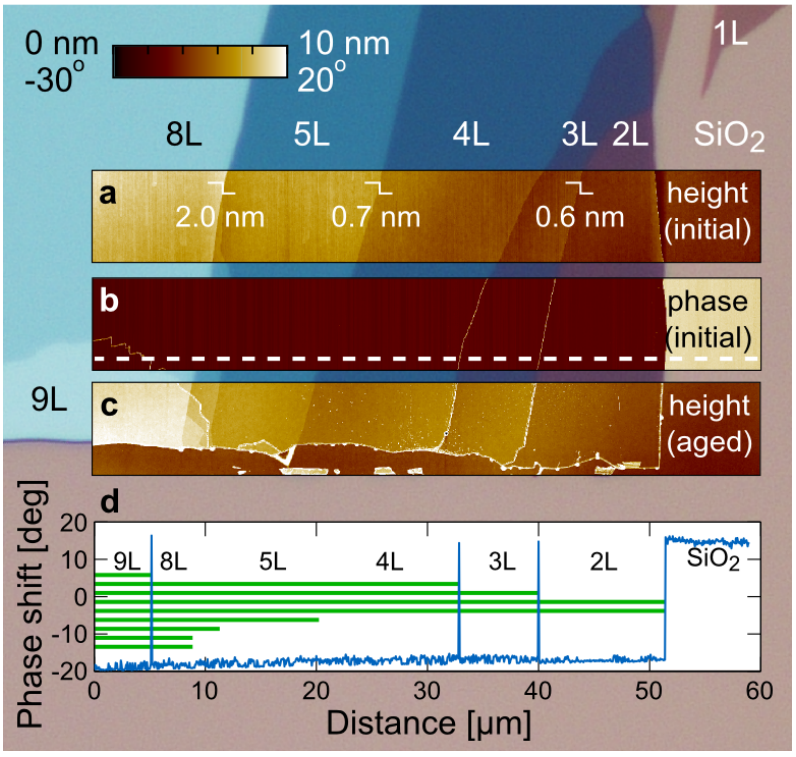


Figure 6.1: *Optical micrograph of a staircase WSe_2 flake of one to nine layers. The micrograph is overlaid with (**a**) topography and (**b**) phase-contrast AFM of the pristine flake, and (**c**) topography AFM after four and a half months of exposure to ambient conditions. (**d**) The phase shift along the dashed line in (**b**) is plotted along with a sketch of the presumable order of the layers predicted by the initial phase-contrast AFM.*

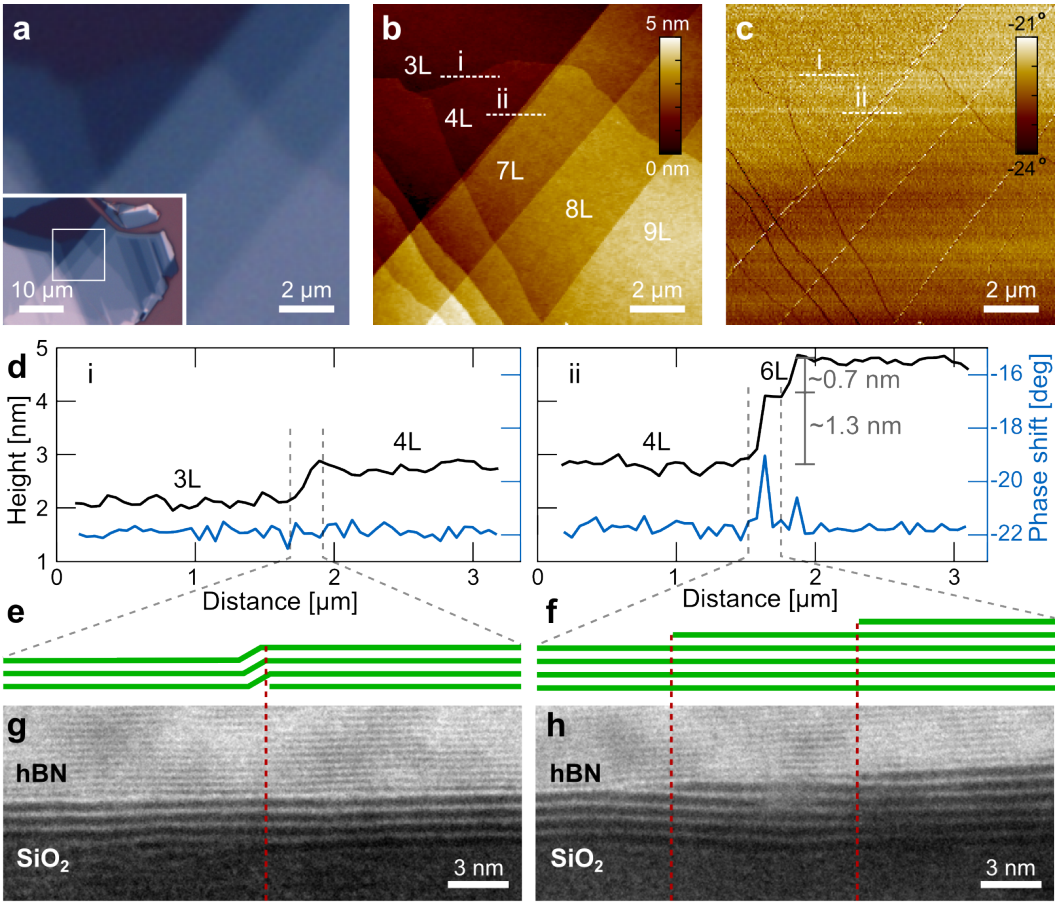


Figure 6.2: *(**a**) Optical micrograph, (**b**) topography and (**c**) phase-contrast AFM of a multilayer WSe_2 flake. (**d**) Height and phase shift line scans of the two steps (i) and (ii), the location of the steps are indicated in the AFM scans of (**b**) and (**c**). (**e**) Sketch of the covered step (i) and (**g**) cross-section TEM micrograph of the step. A hBN flake is dropped-down on-top of the WSe_2 flake to protect the WSe_2 during the sample preparation for cross-sectional TEM. (**f**) Sketch of the exposed steps (ii) from four to six layers and (**h**) cross-section TEM micrograph of the steps.*

in ozone [136], with the oxidation starting at the edges of the flake. In tapping mode AFM the phase-contrast displays variations in surface properties such as elasticity, adhesion and friction [137]. The phase-contrast, at the exposed steps in the initial AFM, is likely due to edge chemistry/compositional variations as a result of fast degradation of the flake.

The correlation between phase-contrast and long-term stability strongly indicates that the difference between the steps is whether they are protected or not. The phase-contrast along with the typography AFM image gives an unambiguous picture of the precise arrangement of the layers in the flake as illustrated in Fig. 6.1d. Here a line scan of the phase-contrast has been overlaid with an illustration of the layer order, to clearly show the narrow spikes in signal occurring at the exposed edges. The phase imaging was done with two different atomic force microscopes on the same flake with similar results.

The relation between the phase-contrast AFM and the order of the layers was confirmed by cross-sectional TEM. The TEM inspection was performed in a Tecnai T20 G^2 microscope operated at 200 kV. Fig. 6.2a-c displays a WSe_2 flake inspected by both AFM and cross-sectional TEM. A covered (i) and an exposed (ii) edge are located in the AFM scan. Edge (i) has negligible phase shift while edge (ii) shows a notable phase shift, while both steps are

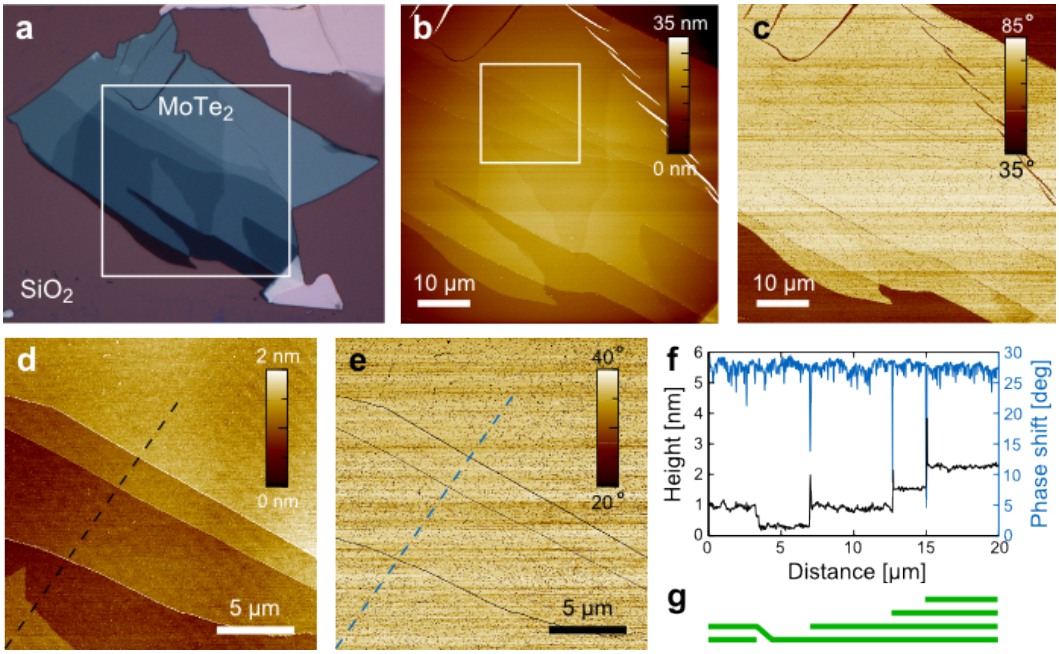


Figure 6.3: *Inspection of a $MoTe_2$ flake. (**a**) Optical micrograph, (**b**) topography and (**c**) phase-contrast AFM of a mechanically exfoliated flake. Zoomed (**d**) topography and (**e**) phase-contrast AFM shows exposed and covered edges. (**f**) The average height and phase shift over 25 lines indicated with dashed lines in (**d**) and (**e**), (**g**) schematic of the order of the layers along the line.*

clearly visible in the topographic AFM images. Line scans of height and phase shift across the two steps are shown in Fig. 6.2d, with (i) and (ii) corresponding again to covered and exposed edges, respectively, see illustrations in 6.2e-f. To prepare the flake for TEM cross-sectional imaging, a hBN flake was dropped down on top of the WSe_2 employing the pick-up transfer method, see Sec. 4.2 [20], in order to protect the WSe_2 during sectioning. A cross-sectional plane including both edge (i) and (ii) was milled out by focused ion beam milling (FIB) and placed on an Omnigrid®. The TEM images show an atomically clean interface between the WSe_2 flake and the protecting hBN flake.[1] Fig. 6.2g-h displayed the cross-sectional TEM images of the two steps. The difference in interlayer spacing of the hBN and the WSe_2 is easily recognised, likewise is the difference in Z-contrast between the lighter B and N atoms and the heavier W and Se atoms clear. Moreover, the appearance of the two edges (i) and (ii) in the cross-sectional TEM confirm the order predicted by the phase-contrast AFM, see Fig. 6.2g-h. The phase-shift of the tapping mode AFM in conjunction with height scans can therefore be used to determine the arrangement of buried layers and edges in multilayer WSe_2 flakes.

Mechanically exfoliated flakes of $MoTe_2$ and MoS_2 have also been inspected by AFM within few hours after exfoliation. Optical images and AFM data for a $MoTe_2$ flake are displayed in Fig. 6.3. Previous studies [138] propose that O_2 mostly interact with intrinsic Te-defects in the $MoTe_2$ lattice leading to degradation within a time scale of days under ambient conditions. In accordance with this, the $MoTe_2$ flake was found to decay rapidly in ambient conditions, with particle-like structures observable by AFM inspection. During scanning, the movement of the AFM needle across the surface tends to move the particles and lead to particle accumulating at the exposed edges. This is seen as an increase in the height at the exposed edges where a phase shift is observed, see Fig. 6.3d-f. The phase shift at the exposed edges may therefore be

[1] Patrick Rebsdorf Whelan prepared the cross-section WSe_2 sample and Timothy J. Booth performed the TEM inspection.

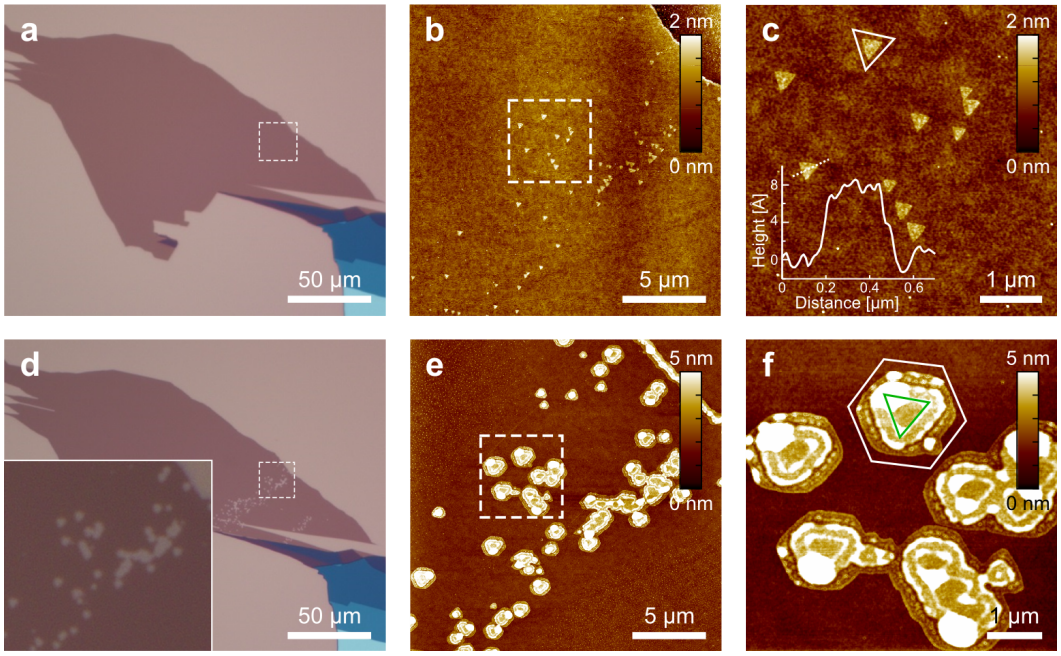


Figure 6.4: *(**a**-**c**) Optical and topography AFM micrographs of the just exfoliated monolayer WSe_2 and (**d**-**f**) after four and a half months under ambient conditions. The dashed square indicate the areas inspected by AFM. Small triangular second layers are observed under the large monolayer. A line scan across a triangle is included in (**c**). The triangles evolve into larger hexagonal holes over time.*

a result of the particles, as the tip to sample contact area increases then the AFM needle moves over the particle and thereby changes the adhesion which induce a phase shift. The order of the layers along the line in Fig. 6.3d,e are predicted from the AFM scans and illustrated with a scheme in Fig. 6.3g. However, the fast degradation of the $MoTe_2$ makes it unfavourable to perform time-consuming AFM scans of the flake.

The MoS_2 flakes also show some difference between steps, however, not as pronounced as for the WSe_2, and scans are not shown here.

6.1.2 Degradation of WSe_2

Degradation of the WSe_2 flake appears at the exposed edges and at defects already present in the flake before or created during exfoliation. Fig. 6.4 show optical and AFM micrographs of a large monolayer WSe_2 flake close to the staircase WSe_2 flake. The monolayer was inspected both after exfoliation and after exposure to ambient conditions for four and a half month. The initial AFM of the monolayer flake revealed small co-oriented triangles. The height of the triangles matches that of a monolayer, see inset of line scan across in Fig. 6.4c. While kept exposed to ambient conditions the triangles grow in size and eventually become visible by optical microscopy, see Fig. 6.4d. AFM scans reveal a similar structure of all the holes; there is a triangular rim in the inner part of the hole, at which a large particle is located at one of the corners, and the outer part has a hexagonal shape, see Fig. 6.4e and f.

The bulk WSe_2 crystal used for mechanically exfoliation is grown synthetically, and the triangles may therefore be a result of second layer growth at defects, as for CVD grown graphene. CVD growth of WSe_2 has previously been shown to yield triangular flakes [139].

Evolution of the ageing of the one to nine layer flakes from Fig. 6.1 is displayed in Fig. 6.5, with optical and topography AFM micrograph from after two weeks, four and a half months and six months are shown. There are no visible changes after two weeks, but degradation of

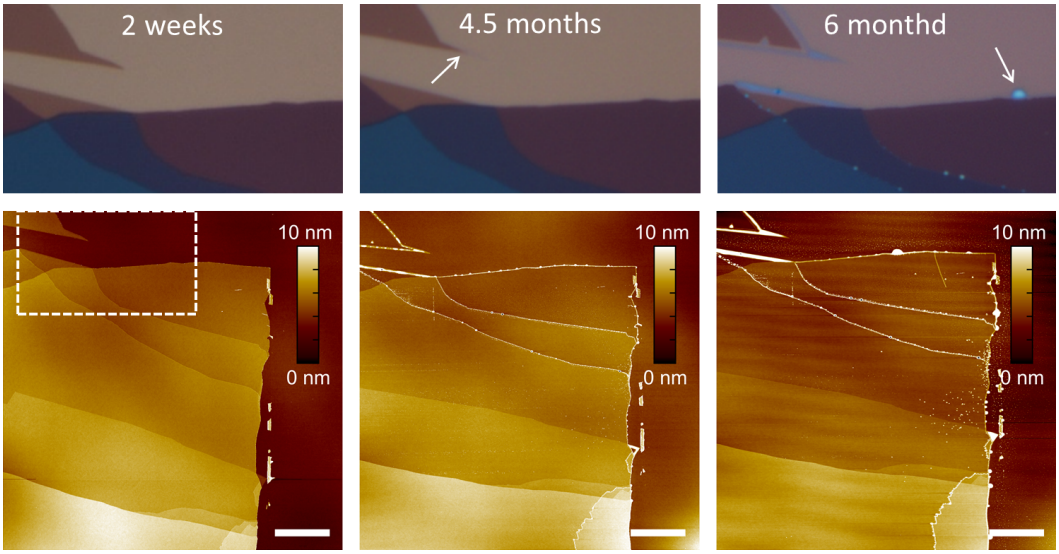


Figure 6.5: *Evolution of WSe_2 flake over a six months period while stored under ambient conditions. Optical and AFM micrograph reveals degradation of the flake. After two weeks the flake appears almost as after exfoliation, while after four and a half months the narrow part of the monolayer in the top is optically smaller, and degradation at some of the steps and of the outer edge of the flake appears. At six months the degradation has advanced and large particles are visible. All scale bars are 10 μm.*

exposed edges are clearly present after four and a half months. After six months the degraded WSe_2 has accumulated into blue particles and contamination appears on the SiO_2 substrate in the proximity of the flake. Furthermore, the degradation is also seen at the monolayer. The vertex in the top left has become significantly more narrow after four and a half months, marked with a circle in the optical image, and has disappeared after six months. No degradation is observed at the covered steps.

To summarise, it have here been shown that phase-contrast and topographic AFM together allows a detailed understanding of the layer structure arrangement of multilayer TMD materials. This permit fabrication of devices where edges can be chosen to be protected or exposed at will. TMDs flakes are not as staple as graphene flakes are, and especially the edges of the flakes degrade over time. However, the degradation of WSe_2 crystals in ambient conditions is found very efficiently halted by being covered with layers of the same material.

6.2 Stencil Devices

Stencil devices were made with WSe_2 flakes to explore the stability of the flakes upon measurements and exposure to ambient conditions. Stencil lithography requires relatively large flakes, as the smallest mask used here yields a channel length of 11 µm, and the flakes needs to be larger than this to have space for alignment. WSe_2 is one of the TMDs that relatively easily yields large mono- to few-layer flakes with scotch tape exfoliation. Furthermore, WSe_2 is also relatively stable under ambient conditions as seen in the previous section, and stencil device fabrication was therefore feasible. Two types of stencil devices were fabricated and measured upon; WSe_2 stencil devices with metal deposited directly on the flake and WSe_2 devices with intermediate graphene contacts.

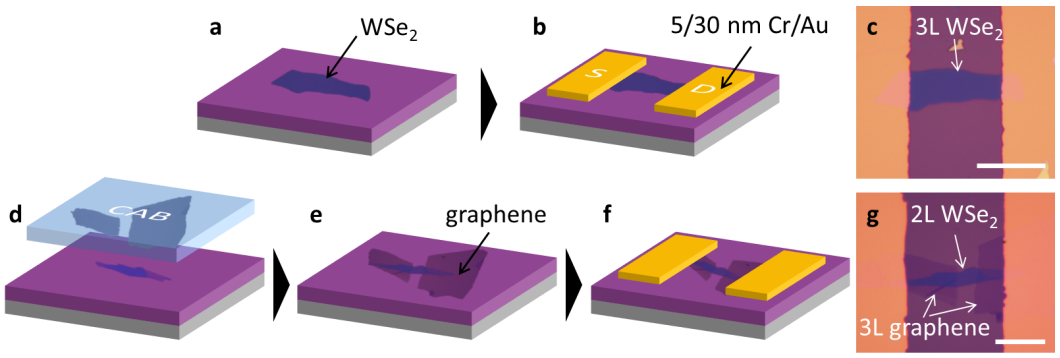


Figure 6.6: *WSe_2 stencil device fabrication.* (**a**)-(**c**) *Stencil devices with metal contacts. The active channel is kept pristine and the metal is deposited directly on the WSe_2 flake.* (**d**)-(**g**) *Stencil devices with intermediate graphene contacts,* (**d**) *graphene flakes are transferred onto the WSe_2 crystal with CAB, the WSe_2 channel is in contact with the CAB and solvents.* (**f**) *Contacts are deposited through a stencil mask onto the graphene. The WSe_2 flake is not in direct contact with the metal. Scale bars in* (**c**) *and* (**g**) *are 20 µm.*

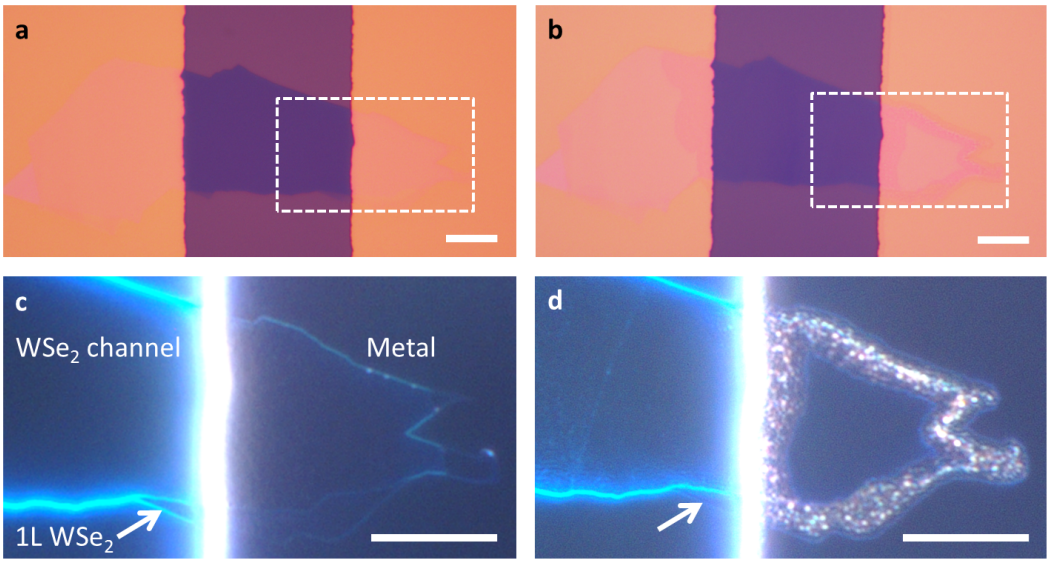


Figure 6.7: *Optical bright and dark field micrographs of a bilayer WSe_2 stencil device* (**a**) *and* (**c**) *a week after fabrication and* (**b**) *and* (**d**) *after three months under ambient conditions. The squares of the bright field frame the area shown in the dark field micrographs of* (**c**) *and* (**d**)*. Arrows indicate a small monolayer region which degrades over time. The edge of WSe_2 under the metal is degrading radically. The scale bars are 10 µm.*

6.2.1 WSe_2 with Metal Top Contacts

Six stencil devices of WSe_2 flakes were fabricated as illustrated in Fig. 6.6a-c. Flakes of WSe_2 were mechanically exfoliated with scotch tape onto a substrate of silicon with 300 nm of thermally grown SiO_2. Metal contacts of 2 nm/30 nm Cr/Au were deposited directly on the flake through the stencil mask. The conditions of the device channel are as close to the just exfoliated WSe_2 flakes as possible, since no polymers or chemicals are involved in the fabrication [46].

The devices were inspected with optical dark and bright field microscopy after metal deposition and after exposure to ambient conditions, see example of bilayer WSe_2 stencil device in

Fig. 6.7. No sign of contamination or defects in the channel or under the electrodes are visible under dark field illumination of the as-fabricated devices. On the contrary, particles and stripes are visible in the device channel after three months under ambient conditions, and regions of monolayers seem to be almost gone, as indicated by arrows in Fig. 6.7b, d. Additionally, four out of the six devices show clear degradation under the metal contacts, especially at the edges of the flakes, and at the edges of the metal contacts, as see the device in Fig. 6.7d. The two devices, which did not show optical degradation, were devices with WSe_2 flakes of three and approximately six layers, and the devices showing clear degradation all were with channels of bi- or trilayer WSe_2 flakes.

Electrical characterisation of the devices took place right after deposition of the metal and after exposure to ambient conditions for one to 14 weeks. All measurements were performed at the probe station and under ambient conditions. Current-voltage characteristics (I-V measurements) and field-effect measurements (gate sweeps) were performed on the stencil devices. The source-drain voltage was swept between $-10\,\mathrm{V}$ and $10\,\mathrm{V}$ at various back gate voltages in the range from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$ (only $-100\,\mathrm{V}$, $-50\,\mathrm{V}$ and $0\,\mathrm{V}$ is plotted in Fig. 6.8). I-V curves from for a device with optically visible degradation are plotted in Fig. 6.8a-b, and I-V curves for a device with no optical degradation is plotted in Fig. 6.8c-d. All initial measurements on the stencil devices showed hole transport and ohmic or close to ohmic behaviour at high negative gate voltages, and a diode-like behaviour is observed in the I-V measurements at gate voltages close to the top of the valence band. Qualitatively, the I-V characteristics for devices with no optical degradation do not change over time, Fig. 6.8c-d. Change in mobility and doping lead to a decrease in resistance of the aged device, but the behaviour remains ohmic. On the other hand, the devices showing degradation optically also tend to have radical changes in the I-V measurements becoming diode-like even at high negative gate voltage for the edges device, see Fig. 6.8a-b.

Examples of field-effect measurements are shown in Fig. 6.9 for the approximately six layer WSe_2 stencil device. This device did not show degradation optically nor changes in the I-V characteristics, inset in Fig. 6.9b displays an optical micrograph of the device. The device was measured right after metal deposition of the contacts, referred to as the initial measurement. Initial measurements of the source-drain current and conductance at various bias voltages are plotted as a function of the applied gate voltage in Fig. 6.9a-b. The current increased as the applied bias, V_{SD}, is increased. The curves for the low V_{SD} collapse on to a single curve in the conductance plot, as expected from the linear I-V characteristics. The measurement with $V_{SD} = 1\,\mathrm{V}$ has a higher conductance indicating that the large source-drain bias helps to overcome a barrier in the system. Fig. 6.9c-d show the resistance and conductance of the device at the initial measurement and at measurements after one week and six weeks of exposure to ambient conditions. Hysteresis is present in the measurements, arrows in Fig. 6.9d show the sweep direction of the measurement after six weeks. The mobilities listed in Fig. 6.9d are the highest of the forward sweeps and the highest of the backward sweeps.

Mobilities extracted from field-effect measurements were found to be in the range of $5\,\mathrm{cm}^2/\mathrm{Vs}$ to $60\,\mathrm{cm}^2/\mathrm{Vs}$ for all the WSe_2 stencil devices with metal top contacts. These mobilities are not astounding and are most likely considerably underestimated as the measurements also include the contact resistance, which furthermore is expected to change over time due to the observed degradation and changes in the I-V characteristics. In literature, the field-effect mobility of WSe_2 have been observed to increase with flake thickness until $\sim$12 layers of WSe_2 and then it starts to decrease. With a two-terminal field-effect mobilities of $350\,\mathrm{cm}^2/\mathrm{Vs}$ for the $\sim$12 layer WSe_2 device at room temperature with Ti/Au contacts [140].

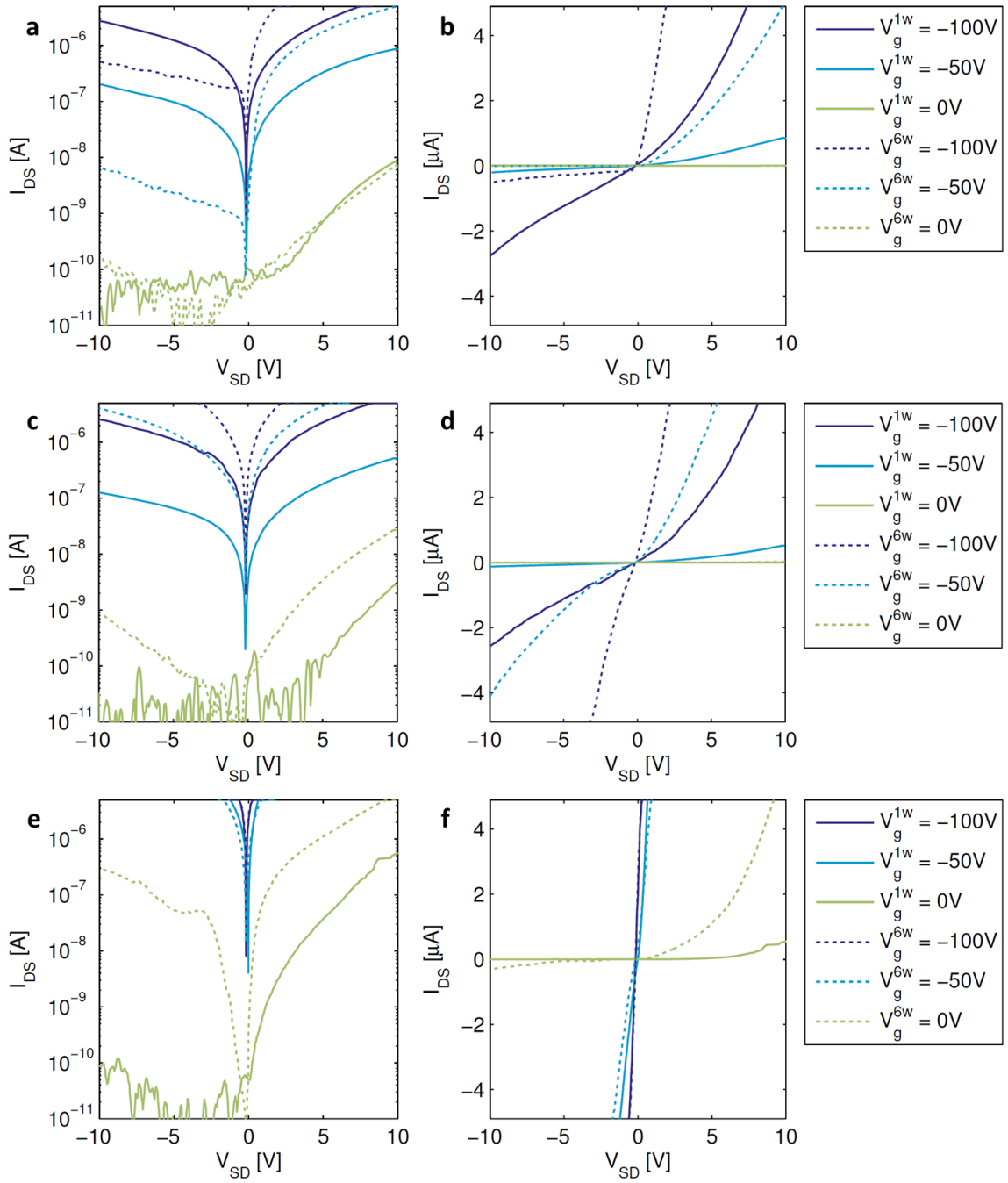


Figure 6.8: *I-V characteristics after one and six weeks exposure to ambient conditions, plotted both on a logarithmic (LHS) and a linear (RHS) scale. Plots of* (**a**)-(**b**) *are from* WSe_2 *stencil device with metal top contacts where degradation are visible, the I-V characteristics change from close to ohmic after one week to diode-like after six weeks.* (**c**)-(**d**) *also from a* WSe_2 *stencil device with metal top contacts, but devices without degradation, the behaviour stays close to ohmic.* (**e**)-(**f**) *I-V characteristics from* WSe_2 *stencil with metal on intermediate graphene contacts. Little change over time, ohmic behaviour and lower resistance is observed.*

6.2.2 WSe_2 with Graphene Contacted

Devices with intermediate graphene contacts were fabricated as the metal contacts had shown to react with the thin WSe_2 flakes over time. Furthermore, the work function of graphene, and

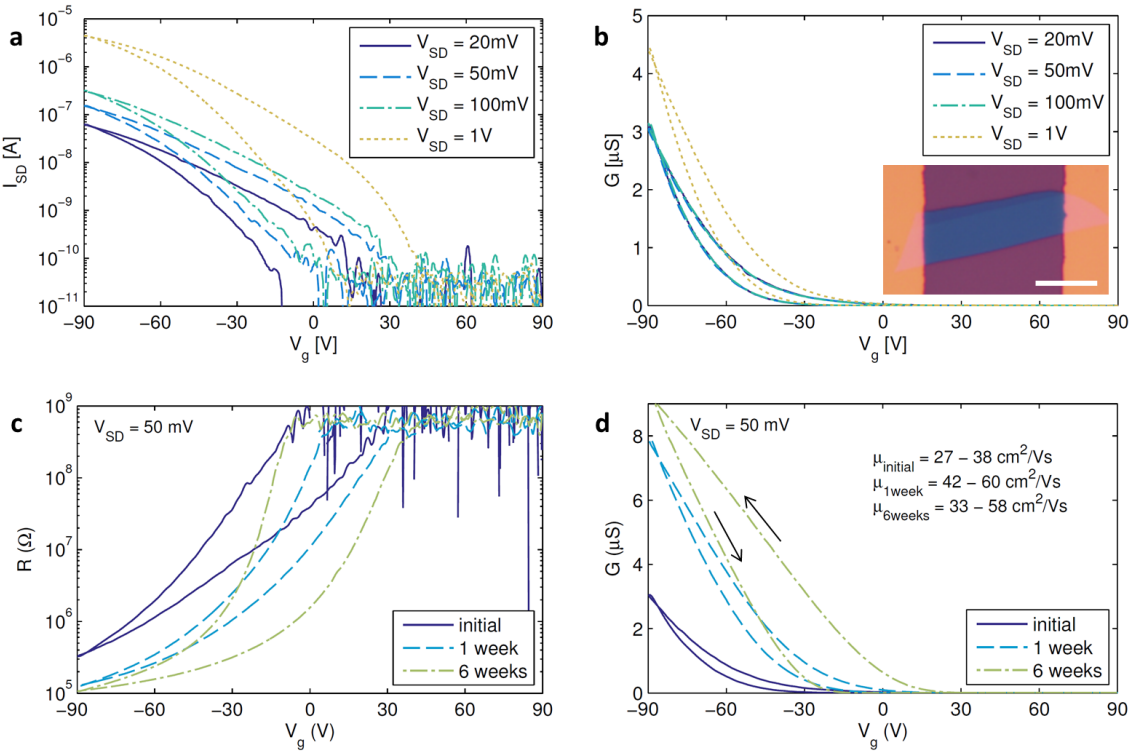


Figure 6.9: *Field-effect measurements from a approximately six layer thick WSe_2 stencil device with metal top contacts on a dielectric of 300 nm SiO_2. Inset in (**b**) displays optical micrograph of the device, scale bar is 10 μm. Plots of initial (**a**) source-drain current and (**b**) conductance as function of gate voltage for four values of V_{SD}. (**c**) Resistance and (**d**) conductance versus gate voltage at the initial measurements, after a week and after six weeks exposure to ambient conditions. Full sweeps are plotted and a range of the two-terminal mobilites are listed due to hysteresis. The measurements of (**c**) and (**d**) are perforemed with at a source-drain voltage of 50 mV. All measurements are at carried out at room temperature.*

ultimately the contact resistance, is tunable by electrostatic gating, see Sec. 2.3. Intermediate graphene contacts were transferred with CAB on top of the WSe_2 both to protect the TMD from direct contact with the metal and to exploit the tunability of the graphene. Fabrication of these devices is as follows; first two chips of exfoliated graphene are prepared and graphene flakes of two to three layers are located optically. CAB is then spun on one of the graphene chips, and flakes from this chip are transferred to the other graphene chip. Flakes of the same thickness are matched and placed with a separation of 5 μm to 20 μm, which later becomes the device channel. The two graphene flakes are then again lifted up with the CAB and transferred onto the WSe_2 flake which will form the channel. To lift off the CAB with flakes from the substrate, water is used, as it wedges in-between the hydrophilic SiO_2 surface and the hydrophobic CAB. The CAB with graphene flakes is left to dry on a PDMS block attached to a glass slide. The glass slide is mounted at the micro-manipulator, as for vdW assembly, and with this aligned to the target flake without water. Finally, metal contacts of 2 nm/30 nm Cr/Au were deposited through the stencil mask onto the graphene, see Fig. 6.6d-g. Four graphene contacted devices were fabricated, two devices with bilayer WSe_2, one with trilayer and one with fourlayer WSe_2. The time evolution of the WSe_2 devices characteristics, with intermediate contacted graphene, is significantly more consistent compared to the devices with pure metal contacts. The I-V characteristics is ohmic at high negative gate voltages (−100 V), and diode-like closer to the top of the valence band, both at the initial measurements and after one, six and 14 weeks of

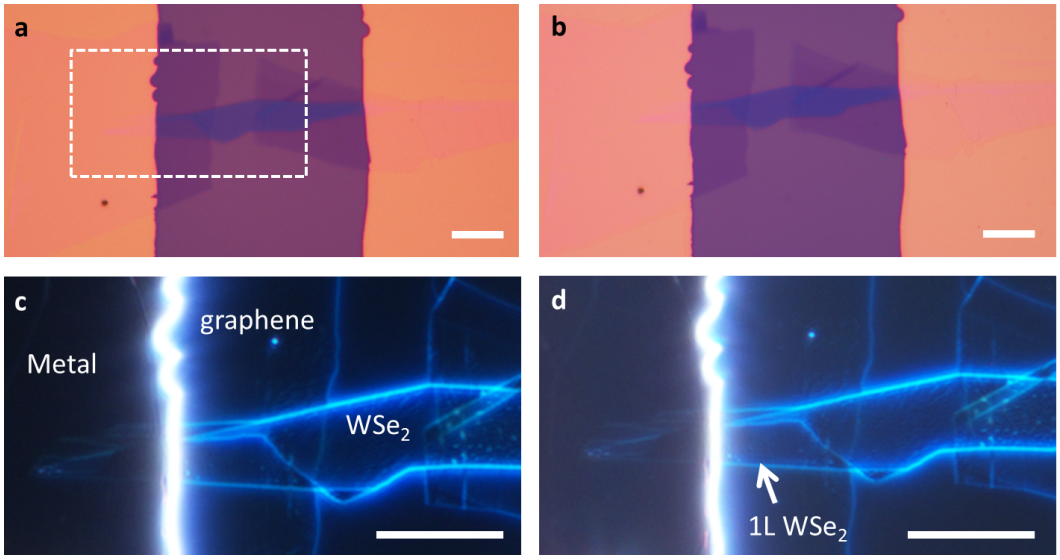


Figure 6.10: *Bright and dark field optical micrographs of a graphene contacted bilayer WSe_2 flake. (**a**) and (**c**) One week after fabrication, (**b**) and (**d**) after three months under ambient contidions. No defects are visible and even a monolayer WSe_2 under the left graphene contact in (**d**) stays intact. The scale bars are 10 μm.*

exposure to ambient conditions. A small change is observed in the I-V characteristics as the device gets slightly more p-doped over time. I-V characteristics from after one and after six weeks are plotted in Fig. 6.8e-f for comparison with the pure metal contacted stencil device. The mobility increases over time, but this increase is attributed to the change in doping, as the mobility does not reach a constant value. The two-terminal mobilities were calculated and found to be in the range of 5 cm^2/Vs to 40 cm^2/Vs. A great difference from the pure metal top contact was that the two WSe_2 devices with thicker flakes and intermediate graphene contacts showed ambipolar behaviour.

6.3 hBN-Encapsulated TMDS with Graphene Contacts

Cleanroom fabrication and electrical characterisation have been equally distributed between Bjerke Sørensen Jessen and myself. Filippo Pizzocchero has assembled the stacks.

Since TMDs often are highly sensitive to ambient conditions compared to graphene [141, 142], hBN-encapsulation is favourable, and encapsulated devices have therefore been fabricated. Fully hBN-encapsulation dose not only provide a shielding from the environment but it also provides a flat substrate free of dangling bonds and charge traps. Electrical contacting of hBN-encapsulated TMDs is a great challenge. The 1D edge contacts which works well with graphene can, in our experience, not be applied to TMDs, even though theoretical work implies that edge-contacts should be favourable over top contacts [53, 143]. Different solutions have been employed in literature. Contacts to hBN-encapsulated TMDs have been made by timing the etch time so mainly the top-hBN flake is etched. For this an O_2 plasma, which had a slower etch rate in the TMDs compared to the hBN, has been used [144]. This approach works for thick multilayer TMD flakes; however, for mono- to a few-layere flakes the timing becomes very critical and essentially unfeasible. Contacts have also been created by using pre-patterned top-hBN [145] creating pure top contacts to the TMDs.

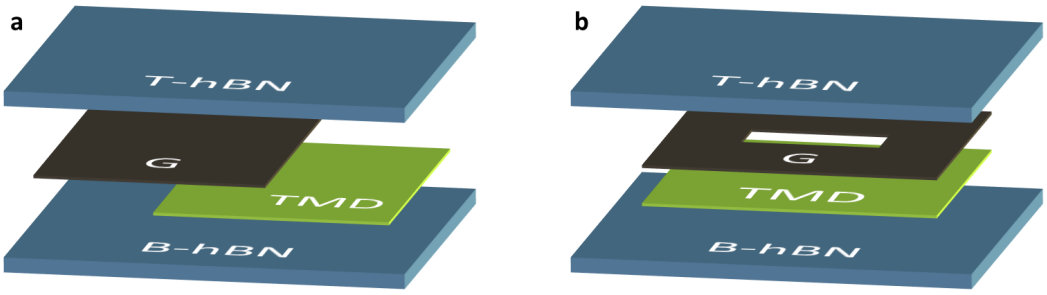


Figure 6.11: *Exploded scheme illustrating the flakes involved in a stack of hBN-encapsulated TMD (**a**) with pristine graphene contacts, and (**b**) with pre-patterned graphene contacts. The stacks are assembled from the top and down, first picking up the top-hBN then the graphene followed by the TMD and the hBN/graphene/TMD is then finally dropped down on the bottom-hBN.*

6.3.1 Fabrication

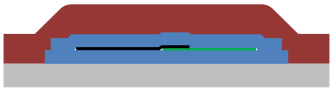
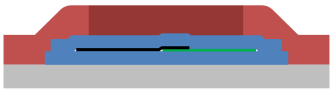
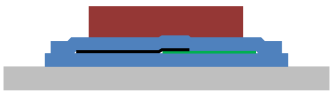
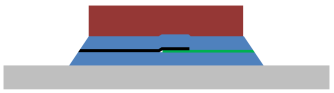
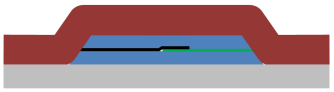
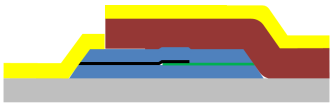
In this work, graphene is used as a intermediate 2D contact to hBN-encapsulated MoS_2, $MoTe_2$ and WSe_2, as shown for MoS_2 in [23, 146]. Graphene contacts of either pristine or pre-patterned graphene have here been used. If contacts are needed on both side of the device channel, as for a Hall bar geometry, multiple graphene flakes will have to be picked up in order to form graphene electrodes around the perimeter of the TMD [23]. Pre-patterned graphene can be picked-up with the "Hot pick-up" method published in [20]. The great advantage of the pre-patterned contacts is the flexibility, as flakes of graphene can be tailor-made for specific device architectures. For instance, graphene flakes with rectangular holes, as illustrated in Fig. 6.11b, enable fabrication of Hall bar structures. The graphene and TMD are aligned on top of each other so TMD is in the pre-patterned hole of the graphene. The device channel is then designed in the rectangular hole where the stack is hBN/TMD/hBN, and the contacts is then made from the surrounding graphene where the layers of the heterostructure are hBN/graphene/TMD/hBN. Circular designs can be made to test angular dependency in anisotropic 2D crystals such as black phosphorus, see Fig. 4.7c-d.

The shape of the pre-patterned graphene flakes are defined by EBL, and etched with an O_2 plasma. The disadvantage of the pre-patterned graphene electrodes is the unavoidable PMMA residues from the EBL fabrication, which may get trapped in the stack. However, the residues are not considered a great problem since there will not be residues in the area where the graphene is etched away, and the device channel will be in this area. Hence, the active device channel constructed from the TMD is not exposed to any polymer or solvent.

The TMD stacks are constructed by vdW assembly. The top-hBN is first picked up with the PDMS/PPC block on a glass slide and dropped down on a graphene flake at 110 °C, as described in Sec. 4.2. The top-hBN and graphene is then picked up together, aligned to and dropped down on the TMD flake, this is done at a lower temperature (40 °C – 50 °C) to avoid degradation of the TMD flake. A pristine graphene flake will be aligned to the TMD so only a part of the two flakes are overlapping. The overlapped region will form the graphene to TMD contacts and the remaining part of the TMD will become the device channel. Pre-patterned graphene contacts will be aligned according to the design. Finally, the hBN/graphene/TMD is picked up and dropped down on the bottom-hBN for full encapsulation. See schematic of the two types of stacks in Fig. 6.11.

Box 5: hBN/G/TMD/hBN stacks

Fabrication steps from an hBN-encapsulated TMD with graphene contacts to a shaped and contacted device.

Illustration	Step	Parameters
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Post-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Etch	PMMA Descum 5 s O_2/Ar Top-hBN 20 s SF_6 Graphene 20 s O_2/Ar Bottom-hBN 20 s SF_6
	Resist strip	Rinsed in acetone + IPA + N_2 blow-dry
	Resist spin	Pre-bake: 10 min @ 180 °C 4 % PMMA in anisol: spin speed of 1500 rpm, acc. of 500 rpm for 1 min Post-bake: 10 min @ 180 °C
	E-beam exposure	Current: 6 nA Dose: 600-1000 μC/cm^2
	Development	60 s in 3:1 IPA:H_2O 30 s IPA rinse N_2 blow-dry
	Metallisation	5/50 nm of Cr/Au or 2/15/30 nm of Cr/Pd/Au
	Metal lift off	Chip is immersed in heated acetone for approximately 20 minutes

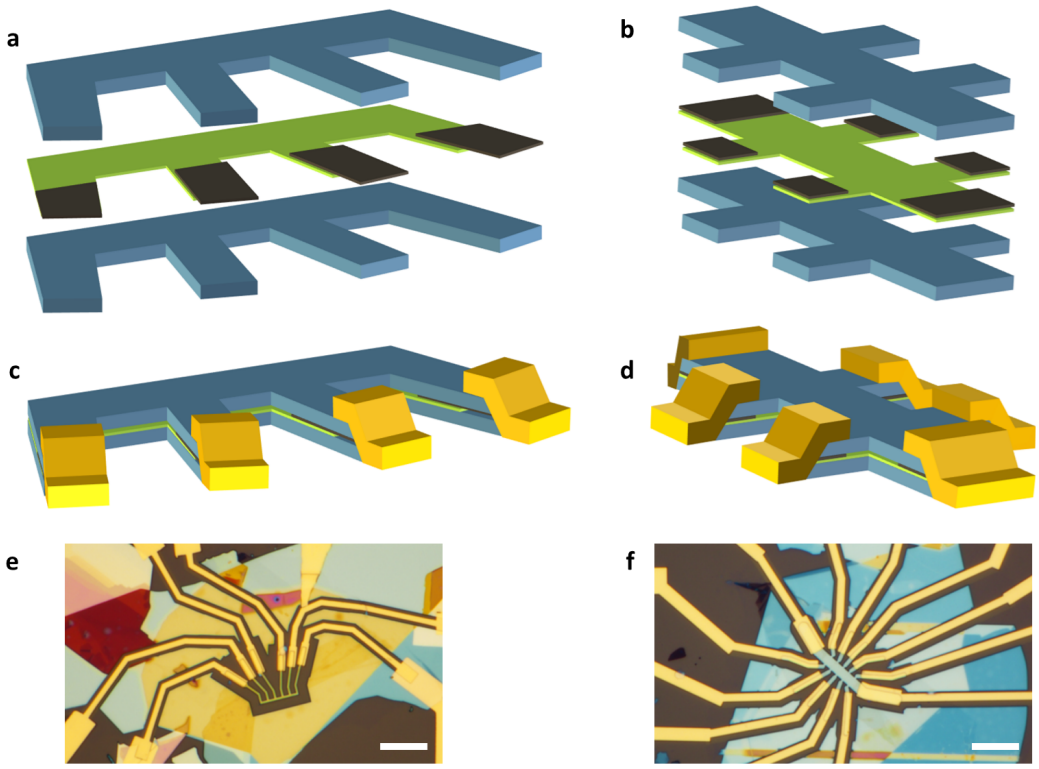


Figure 6.12: *Schematic illustration of hBN/graphene/TMD/hBN stacks after shaping. Illustration of (**a**) a stack with pristine graphene contacts and **b**) a stack with pre-patterned graphene contacts. (**c**)-(**d**) Illustration of the shaped and contacted devices. Optical micrographs of (**e**) TMD device contacted with pristine graphene and (**f**) with pre-patterned graphene. Scale bars are 10 µm.*

The cleanroom process steps from the hBN/graphene/TMD/hBN stack to a shaped and contacted device are outlined in fabrication Box 5. Briefly, the assembled stack is first etched into the desired shape defined by EBL, scheme of etched stacks with pristine and pre-patterned graphene contacts are shown in Fig. 6.12a-b. The 1D edge metal contacts are then made by EBL, metal deposition and lift off, see illustrations of contacted devices are displayed in Fig. 6.12c-d.

6.3.2 Room Temperature Measurements MoS_2 and $MoTe_2$

Several devices of hBN-encapsulated MoS_2, $MoTe_2$ and WSe_2 have been fabricated and characterised electrically. Data from MoS_2 and $MoTe_2$ devices will be presented here. All stacks presented here are assembled under ambient conditions. Assembly in a glove box is obviously favourable especially for the more air sensitive flakes. $MoTe_2$ is one of the lesser stable TMDs, as also observed with AFM inspections in Sec. 6.1. Flakes of $MoTe_2$ were therefore exfoliated, identified with optical microscopy and encapsulated within a short time frame of approximately one to two hours. This was done to limit the exposure to ambient conditions and thereby minimise degradation. The more stable MoS_2 and WSe_2 flakes were encapsulated within one to two day after exfoliation and the flakes ware stored in a vacuum desiccator when possible, again to minimise the degradation.

Mobility data from four-terminal field-effect measurements on five MoS_2 and three $MoTe_2$ devices are listed in Table 6.1, and optical micrographs of the devices are displayed in Fig. 6.13. The hBN-encapsulated TMD devices shown very stable over time. The MoS_2 device A1

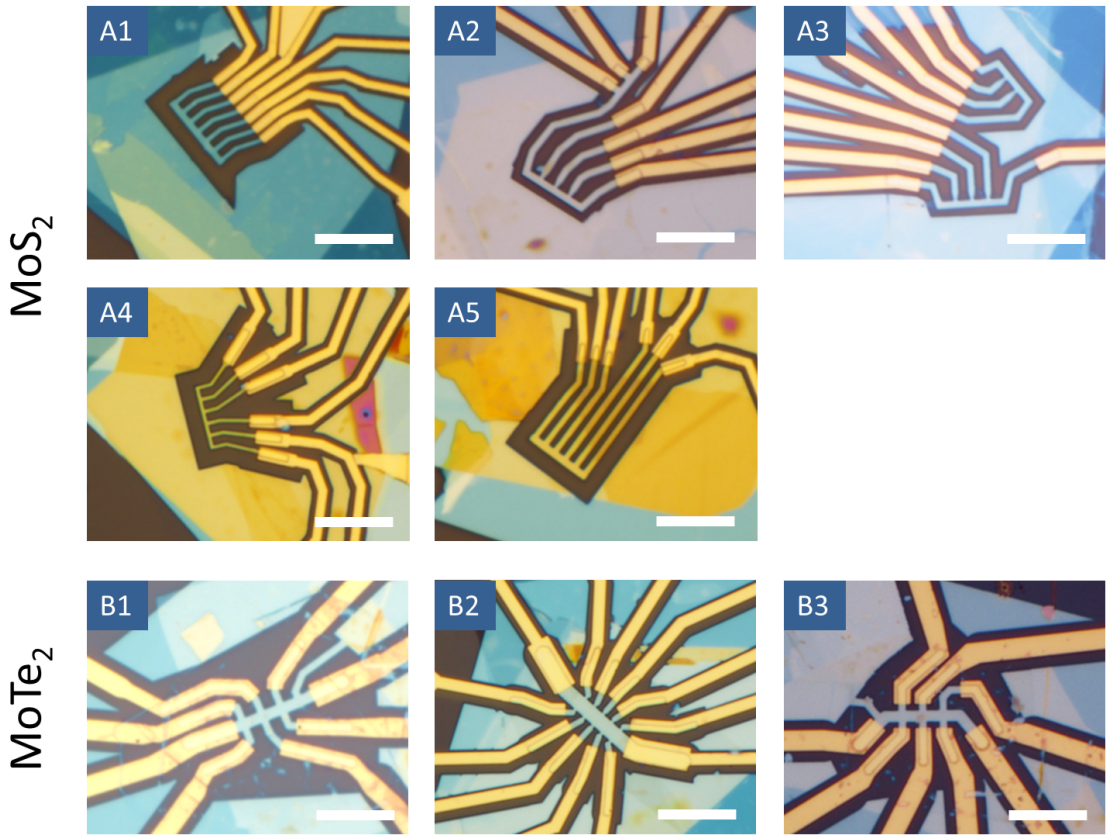


Figure 6.13: *Optical micrographs of the hBN-encapsulated MoS_2 and $MoTe_2$ devices listed in Table 6.1. Device B1 and B3 are with pre-patterned graphene contacts and the renaming devices are fabricated with pristine graphene. Scale bars are 10 μm.*

and the $MoTe_2$ devices B1 were measured just after fabrication and after a year under ambient conditions showing no sign of degradation electrically or optically. The data displayed below in Sec. 6.3.3 and Sec. 6.3.4 are from after a year.

Table 6.1: *Room temperature two-terminal source-drain and four-terminal mobilities for hBN-encapsulated MoS_2 and $MoTe_2$ devices with graphene contacts. Low temperature measurements are performed on devices A1 and B1. Device id and flake thickness of both TMD and graphene are listed, and e/h denote electron/hole transport. Graphene marked with $\star$ are pre-patterned flakes.*

Id	TMD	Graphene	e/h	μ_{SD} [cm^2/Vs]	μ_{4p} [cm^2/Vs]
A1	1L MoS_2	1L	e	8 ± 1	44 ± 2
A2	2L MoS_2	1L	e	18 ± 1	125 ± 20
A3	3L MoS_2	1L	e	22 ± 2	23 ± 2
A4	3L MoS_2	1L	e	8 ± 1	28 ± 7
A5	>4L MoS_2	1L	e	16 ± 1	33 ± 2
B1	2L $MoTe_2$	2L*	h	1.8 ± 0.2	18 ± 1
			e	2.2 ± 0.1	13 ± 1
B2	1L $MoTe_2$	>4L*	h	2.0 ± 0.1	2.5 ± 0.3
B3	2L $MoTe_2$	3L*	h	8 ± 1	13 ± 1

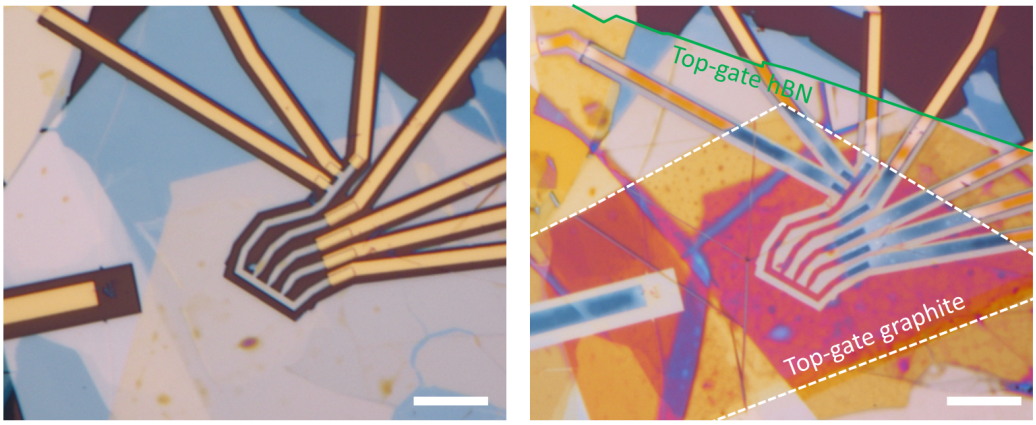


Figure 6.14: *Left: MoS_2 device A2 prior to transfer of graphite top-gate, the metal lead for the top-gate is seen in the bottom left of the optical micrograph. Right: Device after CAB transfer of graphite top-gate and additional hBN flake for gate dielectric. The border of the graphite and hBN flakes are outlined, the graphite is in direct contact with the metal lead with outside the view of the optical micrograph. The scale bars are 10 μm.*

All devices have been characterised by four-terminal measurements using a highly doped silicon back-gate to vary the charge carrier density, furthermore graphite top-gate have been added. The top-gates are constructed by transferring a hBN/graphite heterostructure on top of the fully fabricated device, see Fig. 6.14. The graphite is first transferred onto the hBN and the hBN/graphite heterostructure is then transferred onto the device, all transfer steps are performed with the CAB transfer technique. CAB transfer is used due to its better suitability for rough surfaces compared to vdW assembly.

6.3.3 MoS_2 with Pristine Graphene Contacts

Room to low temperature data from a hBN-encapsulated MoS_2 devices with pristine graphene contacts are presented here. The electrical measurements were performed in the Linkam setup in a nitrogen atmosphere. Both the MoS_2 and the graphene flake are monolayers, employing the tunability of the work function of the monolayer graphene as a contact material to the MoS_2. The device is referred to as device A1, optical micrograph of the device is seen in Fig. 6.16d. A 90 nm SiO_2 and 20 nm hBN flake comprise the dielectric layer between a highly doped silicon back gate and the device channel.

I-V characteristics at room temperature and at low temperature, 78 K, are plotted in Fig. 6.15a-b. I-V sweeps are performed at gate voltages from -10 V to 40 V in steps of 5 V. Linear and a very close to linear behaviour are observed at room temperature and low temperature, respectively. The temperature dependency is illustrated in Fig. 6.15c-d, with the I-V characteristics at $V_g = 0$ V, 20 V and 40 V plotted together for all measured temperatures. There is no strong temperature dependency for the high gate measurements where the channel is in its on-state (20 V and 40 V). There are however a temperature dependency for the I-V measurements close to the off-state $V_g = 0$ V, here a decreasing resistance is observed when the temperature is lowered.

Four-terminal measurements were also performed and key values are plotted in Fig. 6.16. Only electron conduction was observed, and the gate voltage was therefore swept in the range from $V_g = -10$ V, where the channel is off, to $V_g = 40$ V. Gate sweeps were performed for source-drain bias voltages of 0.2 V and 1 V. The current measured between source and drain as a function of the applied back gate is plotted in Fig. 6.16a for the source-drain biases of 0.2 V. Fig. 6.16b display the conductivity from the voltage probes of the four-terminal measurement,

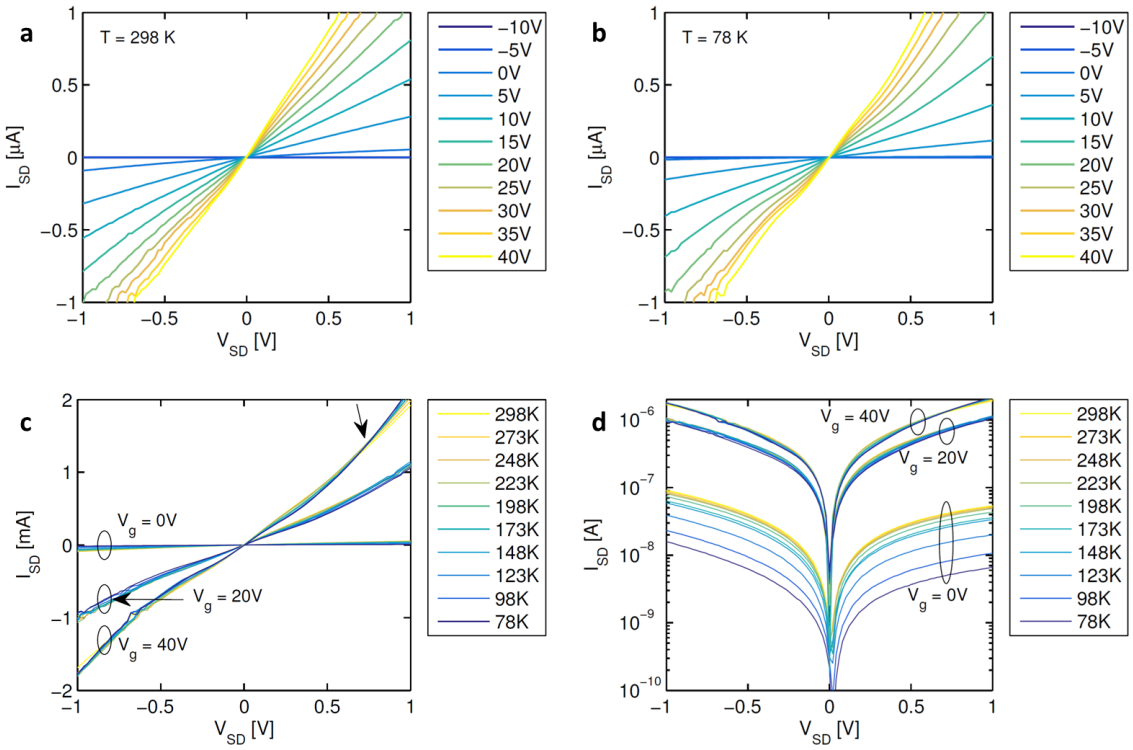


Figure 6.15: *Source-drain I-V characteristic for hBN-encapsulated monolayer MoS_2 contacted with pristine monolayer graphene contacts (device A1). (**a**) and (**b**) I-V measurements for gate voltages of -10 V to 40 V for the two temperature extremes 298 K and 78 K, respectively. Temperature dependency of the I-V characteristic at gate voltages of V_g = 0 V, 20 V and 40 V plotted on (**c**) a linear scale and (**d**) a logarithmic scale.*

the mobility of the devices is calculated from this to be $\sim 44\,\mathrm{cm}^2/\mathrm{Vs}$ at room temperature and increase to close to $200\,\mathrm{cm}^2/\mathrm{Vs}$ at 78 K, the mobility as a function of temperature is plotted in Fig. 6.17. The contact resistance is calculated from the total resistance measured between source and drain, which is the sum of the resistance of the two contacts and the resistance of the channel, hence $R_{tot} = 2R_C + \rho L/w$. The resistivity, ρ, is found from the four-terminal measurement, and the channel dimensions L and w are known from the EBL design. The contact resistance is observed to increasing slightness with decreasing temperature, but is in general very stable. The contact resistance is in the order of MΩ when the channel is switched on and increases radically as the off state is approached. There is modest differentness between the measurements with a source-drain bias of 0.2 V and 1 V, as also seen in the mobilities of Fig. 6.17. The mobility data is fitted by Matthiessen's rule Eq. (2.9)

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \ldots$$

where μ is the measured mobility, μ_C is the mobility limited by charged Coulomb impurity scattering, and $\mu_{ph} \propto T^{-\gamma}$ is the mobility limited phonon scattering. Additional scattering mechanism may be added, however, only phonon and impurity scattering are considered here. The fit to the mobilities yield $\gamma = 1.9$, and a μ_C of $277\,\mathrm{cm}^2/\mathrm{Vs}$ and $300\,\mathrm{cm}^2/\mathrm{Vs}$ for the data measured with $V_{SD} = 0.2$ V and 1 V, respectively.

The ohmic behaviour of the I-V characteristics, see Fig. 6.15, and the lack of a temperature dependency indicates a low if any Schottky barrier at the contacts. However, a large contact resistance is measured in the devices, see Fig. 6.16c, and high contact resistance will often

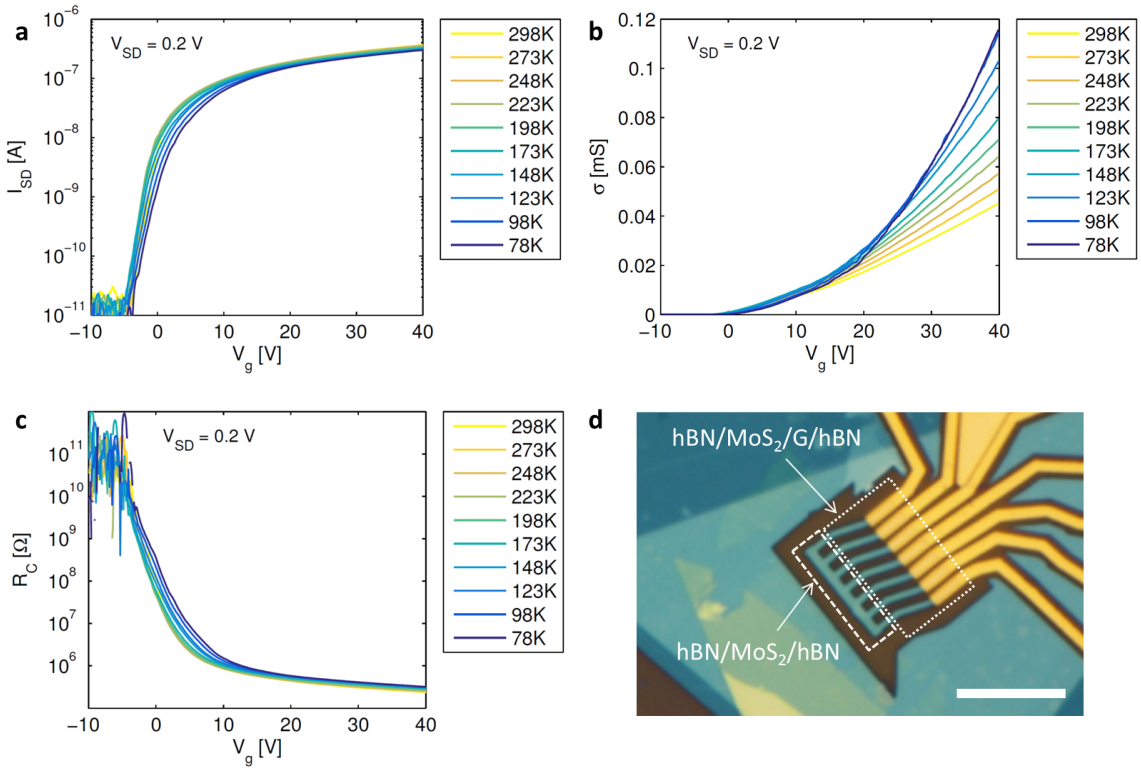


Figure 6.16: *Four-terminal data from hBN-encapsulated monolayer MoS_2 with ohmic monolayer graphene contacts (device A1).* (**a**) *Source-drain current for a bias voltage of 0.2 V and* (**b**) *conductivity of four-terminal measurement at temperatures from 78 K to 298 K.* (**c**) *Plot of contact resistance, where little variation is observed in the whole temperature range measured, R_C is calculated with Eq. (2.15).* (**d**) *Optical micrograph of the device, the area of hBN/MoS_2/graphene/hBN, the 2D contacts, and the area of only hBN/MoS_2/hBN, the device channel, are indicated. Scale bar are 10 µm.*

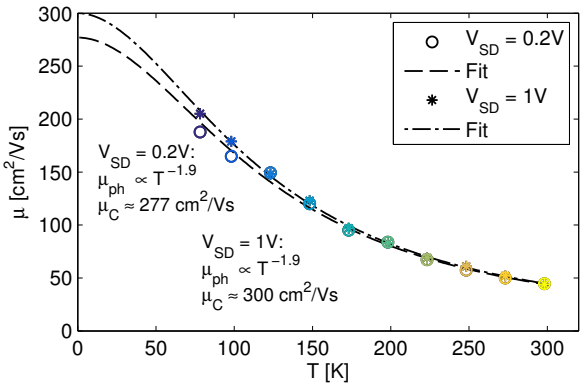


Figure 6.17: *Mobility as function of temperature for MoS_2 device A1. Data from measurements with source-drain bias of 0.2 V and 1 V are plotted. The data is fitted with Matthiessen's rule, fitted values of the γ-factor of the temperature dependency of the phonon scattering, $\mu_{ph} \propto T^{-\gamma}$, and the impurity limited mobility, μ_C, are included in the plot.*

be related to a large Schottky barrier. The 1D contact resistance between the monolayer graphene and the metal leads is known to be small, hundredths of Ω to a few kΩ [20, 21]. It is

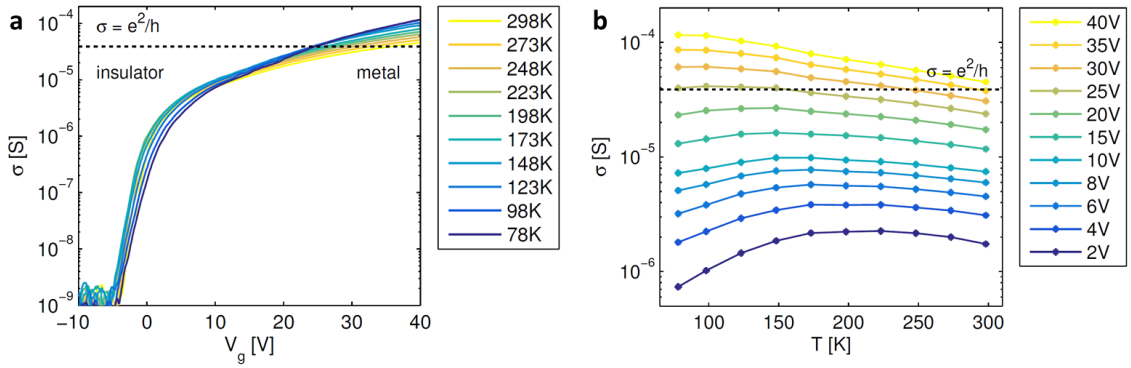


Figure 6.18: *Plot of MIT in hBN-encapsulated monolayer MoS_2 with pristine monolayer graphene contacts. (**a**) Four-terminal conductivity on a logarithmic scale as a function of applied gate voltage. Measurements are performed with an source-drain bias of 0.2 V. (**b**) Four-terminal conductivity as function of temperature at various gate voltages in the on-state from 2 V to 40 V. A line is plotted at the Ioffe-Regel criterion, which predict the MIT to be at $k_F\lambda_{mfp} \approx 1$ equivalent to $\sigma \approx e^2/h$. At high gate voltages ($V_g > 25$ V) a metallic behaviour is observed, the conductivity is decreasing with increasing temperature. Insulating behaviour is observed for temperatures below 200 K and V_g below 25 V where the conductivity decreases with decreasing temperature. Above 200 K the conductivity increases with decreasing temperature for all gate voltages.*

therefore assumed that the large contact resistance is in the graphene to MoS_2 contact. The graphene-TMD contacts resistance will be discussed in more details later in Sec. 6.3.5.

When lowering the temperature, the resistance (conductance) of a metal will decrease (increase), whereas, the resistance (conductance) of an insulator will increase (decrease). A metal-to-insulator transition, MIT, is the transition from a metallic behaviour to an insulating behaviour, here achieved by tuning the charge carrier density. A MIT is observed in the field-effect and I-V measurements of the graphene contacted monolayer MoS_2 device. In Fig. 6.15c an arrow at approximately $V_{SD} = 0.7$ V on the I-V curves measured at a gate voltage of 40 V indicate a transition. The resistance increases for decreasing temperature for bias voltage below this 0.7 V as for an insulator. For bias voltages above 0.7 V the resistance decreases for decreasing temperature as for a metal. The four-terminal conductivity data for measurements with a bias voltage of 0.2 V is plotted in Fig. 6.18. In the metallic regime (at high gate voltages) the conductance is increasing with decreasing temperature, whereas the conductance is decreasing for decreasing temperatures at low gate voltages where the system is in its insulating state, and strong localisations prevails [147, 148].

The Ioffe-Regel criterion for 2D semiconductors predicts the MIT to occur when the criterion $k_F\lambda_{mfp} \approx 1$ is satisfied. $\lambda_{mfp} = \hbar k_F\sigma/(e^2 n)$ is the mean free paths of the charge carrier, and $k_F = \sqrt{2\pi n}$ is the Fermi wave vector for a 2DEG (n is the charge carrier density and σ is the conductivity). Hence, the system is expected to undergo MIT when $\sigma \approx e^2/h$, see plots of the field-effect conductivity along with the Ioffe-Regel criterion in Fig. 6.18. For temperatures below 200 K, the MIT appear at $V_g \approx 25$ V corresponding to a gate induced carrier density of 5×10^{12} cm^{-2}, the conductivity at 25 V is $\sigma(25\,\text{V}) \approx e^2/h$ matching the Ioffe-Regel criterion well, see Fig. 6.18b. A metallic behaviour is observed for all gate voltages at temperatures above 200 K. It is possible to see the MIT due to the high conductivity of the hBN-encapsulated MoS_2, which previously have been reported with use of dual gate geometry [148] and ionic-liquid gating [149] where high carrier densities are obtainable.

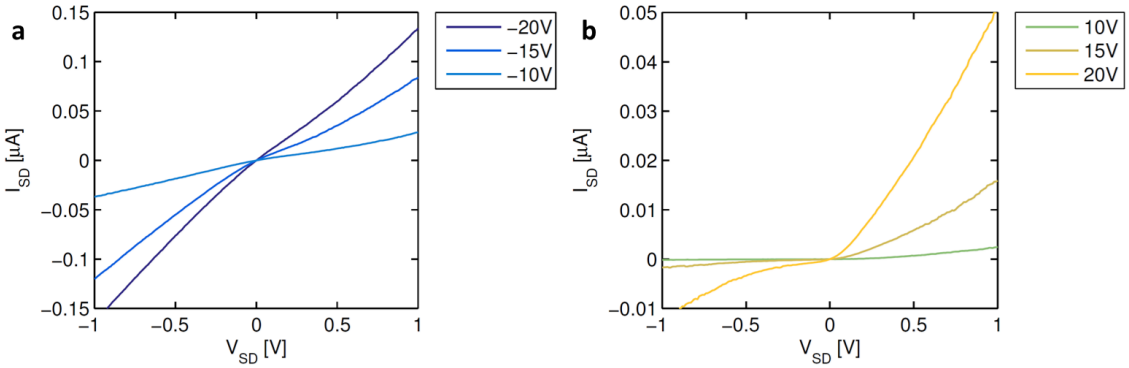


Figure 6.19: *I-V characteristic at room temperature for hBN-encapsulated bilayer $MoTe_2$ contacted with pre-pattern bilayer graphene (device B1). The transport of the devices shows an ambipolar behaviour with hole transport at negative gate voltages (**a**) with a close to ohmic behaviour, and a diode-like characteristic for electron transport at positive gate voltages (**b**).*

6.3.4 $MoTe_2$ with Per-Patterned Graphene Contacts

A vdW heterostructure of bilayer $MoTe_2$ and pre-patterned bilayer graphene contacts was, as the MoS_2 device, measured at temperatures down to 78 K in the Linkam measurements setup. The graphene has a square hole etched before the vdW assembly, and the channel of the final device is located in this square area. Outline of the pre-patterned bilayer graphene and the bilayer $MoTe_2$ flake in Fig. 6.20d are indicating the original borders of the flakes prior to the device fabrication.

Ambipolar behaviour was observed in this device. Fig 6.19 shows the I-V characteristics at room temperature for the $MoTe_2$ device. The I-V curves for negative back gate voltages related to the hole transport are plotted in Fig 6.19a, and the positive gate voltages related to the electron transport are plotted in Fig 6.19b. There is a significant difference in the I-V characteristic, an ohmic behaviour is observed for the hole transport whereas a more diode-like behaviour is observed for the electron transport. The I-V behaviour is ohmic in a large range of source-drain voltages at high positive and negative gate voltages. I-V characteristic in a range of $V_g = \pm 40\,\mathrm{V}$ see plot in Fig. 6.20b.

Source-drain current at a bias voltage of 1 V is plotted in Fig. 6.20a, the evolution with decreasing temperature is markable different for the hole and electron transport. Room temperature four-terminal field-effect mobility of the hole and electrons are 18 $\mathrm{cm}^2/\mathrm{Vs}$ and 13 $\mathrm{cm}^2/\mathrm{Vs}$, respectively. The hole mobility is increasing with decreasing temperature whereas the electron mobility is decreasing with decreasing temperature. The mobilities as a function of temperature are plotted in Fig. 6.20c. Contact resistance at high gate voltage ($V_g = \pm 40\,\mathrm{V}$) for the hole and electron transport increases from $\sim 1\,\mathrm{M\Omega}$ at room temperature to $\sim 7\,\mathrm{M\Omega}$ at 78 K, as seen in the plot of Fig. 6.21. The contact resistance, particularly at the electron transport, increases gradually as the temperature is lowered. The temperature dependency at positive gate voltage may be a result of the non-ohmic behaviour observed in Fig 6.19b. However, it may also be a result of a shift in the doping level.

6.3.5 Discussion

The electrical characterisation yields electron transport in MoS_2 devices and ambipolar transport for $MoTe_2$ devices. Ambipolar behaviour was also observed for device B2 and B3, but no mobility values for the electron transport is included in Table 6.1 as the gate voltage was too high to extract a convincing estimate for the mobility. Hole conductance is observed in all the

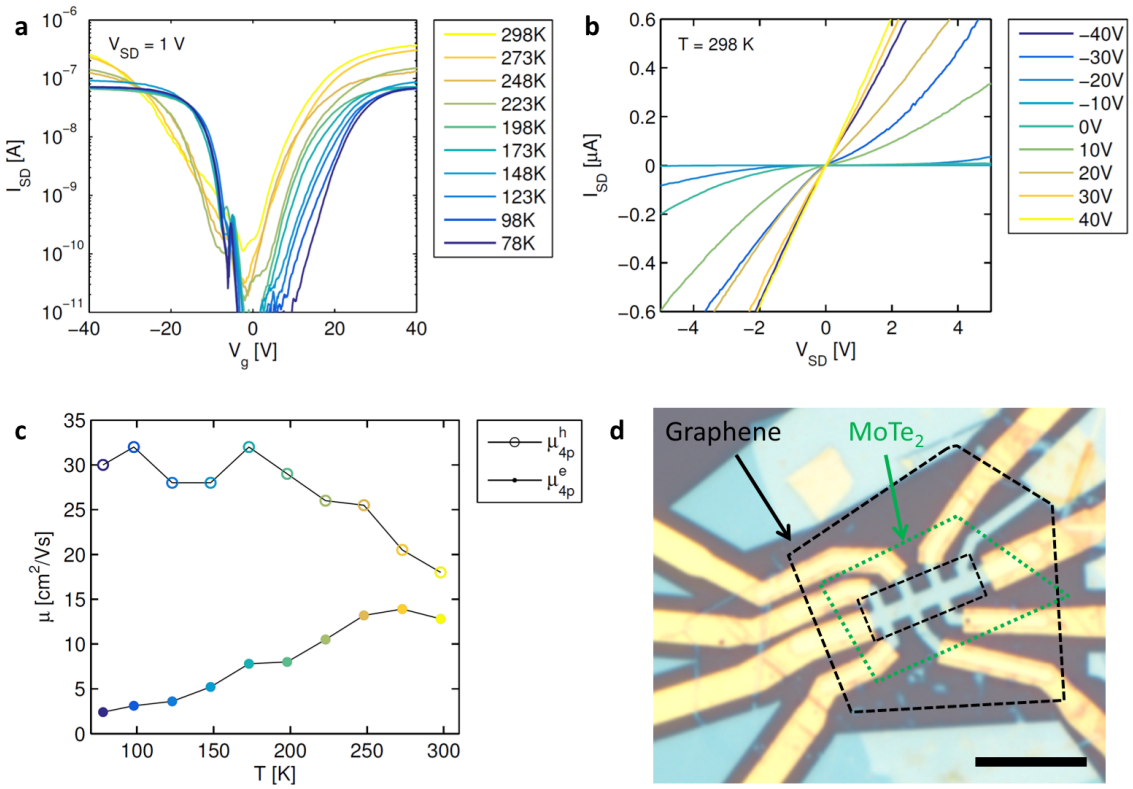


Figure 6.20: *Plots of electrical data from four-terminal field-effect measurements on hBN-encapsulated $MoTe_2$ device B1. (**a**) Source-drain current versus applied gate for a source-drain bias voltage of 1 V. (**b**) Room temperature I-V characteristics, the behaviour is ohmic at high positive and negative bias.(**c**) Four-terminal mobility for electrons and holes as a function of temperature. (**d**) Optical micrograph of the $MoTe_2$ device, the border of the pre-patterned bilayer graphene and bilayer $MoTe_2$ flakes, before shaping the stack into a device, is outlined. The scale bar is 10 μm.*

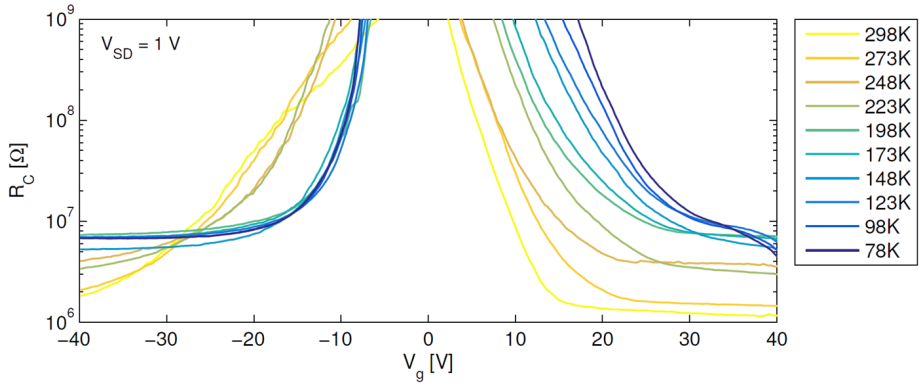


Figure 6.21: *Contact resistance as function of applied back gate voltage of the $MoTe_2$ device B1. The contact resistance is calculated from four-terminal measurements using Eq. (2.15), contact resistance at temperatures from 78 K to 298 K are plotted.*

WSe_2 devices, electron conductance is occasionally observed, mainly for thicker flakes where the bang gap is smaller. This matches well with the presumed alignment of the band structures of the TMDs and that of the tunability of the contacting graphene flakes. The contacts are described in detail in Sec. 2.3, but to summarise. (i) The work function of graphene is tunable,

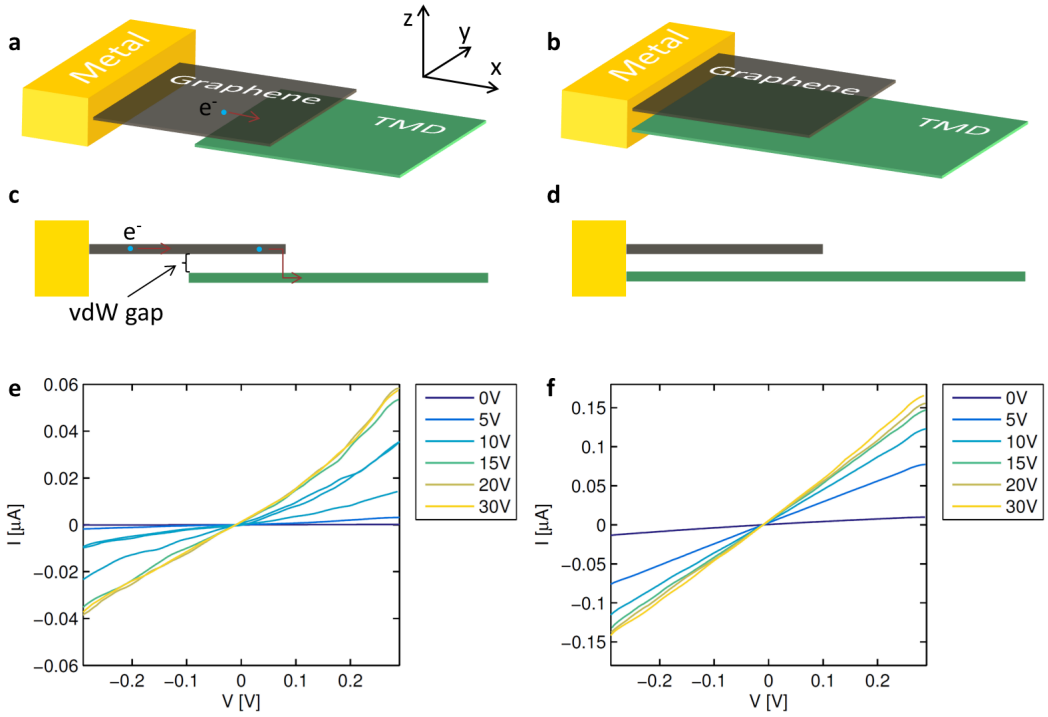


Figure 6.22: *Schematic and measured I-V characteristics of 1D contacts to graphene and 1D contacts to both graphene and the TMD flake. (**a**), (**c**) Charge carriers are injected into the graphene where they travel in the x-y plane before entering the TMD flake. (**b**), (**d**) Charge carriers are injected into both the graphene and the TEM flake sat the 1D contact. (**e**)-(**f**) I-V characteristics of hBN-encapsulated trilayer MoS_2 with pristine monolayer graphene contacts, device A4. This device has both types of contacts fabricated. The I-V characteristics of the (**a**) contacts shows a high contact resistance and a close to linear behaviour (**e**). The (**b**) contacts have a lower resistance and a more linear behaviour (**f**).*

with monolayer being the most tunable. (ii) The tunable range for the graphene is at the conductance band minimum of the MoS_2, in the middle of the band gap of the $MoTe_2$ and also in band gap of WSe_2 but closest to the valence band maximum. See the band alignment in Fig. 2.4. The observed electron transports of MoS_2 and ambipolar transport for $MoTe_2$ is therefore matching well with what was expected.

The mobility measured on the bilayer $MoTe_2$ is reasonably high compared with literature [150, 151], but not at all close to the theoretical limit as defined by acoustic phonen scattering at room temperature [152]. The $MoTe_2$ devices generally yield lower mobilities compared to the MoS_2 devices, even though the phonon limited mobility of MoS_2 should be lower than that of $MoTe_2$ [34, 35]. However, the $MoTe_2$ flakes are significantly more air sensitive and degrade fast under ambient conditions in which the vdW heterostructures were assembled. Assembly in a glove-box would be favourable particularly for the air sensitive crystals.

The contacts have mainly shown ohmic behaviour, but with a very high contact resistance. The high contact resistance is assumed to come from the 2D to 2D flake contact between the graphene and the TMD, as the 1D contact to graphene has a contact resistance three to four orders of magnitude lower. It was discovered that contacts where both the graphene and the TMD were in contact with the metal would have a lower resistance compared to contacts where only the graphene was in contact with the metal. Illustrations of the two contact types are seen in Fig. 6.22a-d. I-V characteristics of the metal to graphene to TMD are plotted in Fig. 6.22e, the resistance is high and the behaviour is less ohmic compared to that of the metal to graphene and TMD plotted in Fig. 6.22f.

The 1D edge contacts do not work with TMDs, it is therefore assumed at the charge carriers will enter the graphene in both contact designs and then pass the physical vdW gap between the graphene and TMD flake to enter the TMD channel of the device. There will therefore be a barrier which the charge carriers have to overcome to enter the TMD.

It was also observed that clean samples with pristine graphene contacts generally would have a higher contact resistance compared to the less clean pre-patterned graphene contacts. This difference in contact resistance may be due to a momentum mismatch as a result of few scattering centres in the clean samples. When the charge carriers are moving in the graphene they will have momentum mainly in the x-y plane, in order to move to an underlying TMD the charge carriers will have to gain momentum in the z-direction. The lower and clearly ohmic behaviour of the I-V characteristics of the contacts in Fig. 6.22b may therefore be a result of carriers entering the TMD while having a momentum in the z-direction, right after the charge injection. However this is yet to be understood fully.

6.4 Summary

In summary, the stability of TMDs exfoliated on SiO_2 has been examined with AFM. Degradation of the WSe_2 crystals in ambient conditions is mainly appearing at exposed edges and is much slower than that of $MoTe_2$ crystals. Furthermore, detection of exposed and covered edges has been demonstrated possible by phase-contrast AFM of the as exfoliated flakes. This detection allows for a detailed understanding of the layer order in multilayer flakes, which may be exploited in device design.

Metal contacts to thin flakes of WSe_2 were found to be unstable and degrade over time from an ohmic to a diode-like behaviour. On the other hand, stencil devices with intermediate graphene contact shown more staples and with prolonged ohmic I-V characteristic.

The architecture of hBN-encapsulated TMDs with graphene contacts has yield devices of high quality and long-term stability. Devices of the highly air-sensitive TMD $MoTe_2$ showed no sign of degradation a year after fabrication, and mobilities comparable with the highest values reported are measured. Moreover, MIT is observed in a monolayer MoS_2 device. The main challenge of the architecture is the high contact resistance, which presumably originate from the 2D graphene to TMD contact within the stack. This contact resistance is still to be fully understood and further explored to make devices with a low contact resistance.

7 Outlook

The main goals in this Ph.D. project have been to fabricate and characterise 2D material devices of high quality and long-term stability, with focus on high yield and cleanliness. Mechanical exfoliation can be applied to both naturally occurring and artificially synthesised bulk crystals of layered materials, and has been used in this project as the exfoliated flakes are of high quality. However, many of the processes and devices architectures can be transferred to CVD grown crystals.

Stencil lithography has, together with a systematic approach, made it possible to distinguish the impact of different processing steps on SiO_2 supported graphene devices. The stencil devices provide a clean, cheap, simple and yet powerful platform for process optimisation and fast testing, which is imperative for fundamental research.

The van der Waals assembly method has been streamlined to increase the device yield, furthermore assembly of pre-patterned flakes and batch fabrication have been made possible. Various techniques and architectures for vdW heterostructures have been developed through the work presented in this thesis. Emphasising on the selective etches, which not only make it possible to stop the etching at a graphene layer, but they also etch very little PMMA and SiO_2. These qualities of the etches make the 1D corner contacts to hBN-encapsulated devices with graphite back-gates and etch of dense nano-patterns into stacks possible. The one step 1D edge contacts with a zero overlap onto the stack have only been developed and made on a few test devices. But the applications for these contacts are quite interesting. They are ideal for top-gating, as no contact metal would shield field-effect gating. They could also be interesting to use for one step contacting of hBN-encapsulated devices without EBL defined edges. Finally, the layer order of exfoliated multilayer TMD flakes has been demonstrated detectable by phase-contrast AFM.

The fabrication has yielded high performances devices with large field-effect mobilities of hBN-encapsulated mono-, bi- and trilayer graphene. The nano-patterning has been made by single-shot E-beam exposures in hBN-encapsulated graphene, these are, to our knowledge, the highest density nano-patterning made by EBL in graphene. In vdW heterostructures with TMDs, high field-effect mobilities have been achieved in the air sensitive $MoTe_2$. Moreover, metal-insulator transition has been observed in a device of fully hBN-encapsulation monolayer MoS_2 with monolayer graphene contacts, with the use of only one gate. High contact resistances have been measured in the hBN-encapsulated TMD devices with intermediate graphene

contacted. This contact resistance is assumed to originate from the graphene to TMD contact, and is a great problem for device performance. The nature of the contact resistance is yet to be fully understood, but various routes may be taken to reduce this resistance. First of all, gates could be fabricated above the graphene to TMD overlap to locally change the work function of the graphene. Nano-patterns could be etched into the contacts before metallisation, to increase the 1D edge length and introduce momentum in the vertical direction for injection of the charge carriers from the graphene flake to the TMD flake. Solving the problem of the contact resistance would make the design of intermediate graphene contacts to hBN-encapsulated 2D materials a universal architecture for systematic screening of architectures of 2D materials.

Fabrication techniques and electrical contact designs have been developed to accommodate architectural demands for 2D layered materials and vdW heterostructure devices. Furthermore, the flexibility of designs has been increased radically by integration of pre-patterned 2D layers in the vdW heterostructures, and post-patterning of ultra-dense nano-patterning has been demonstrated. The patterning gives, together with the vdW assembly and the AFM detection of the layer order in multilayer TMDs, a unique possibility for advance architectures and fabrication of metamaterials and nano-devices with control on an atomic level.

Appendix A

Publication

Graphene antidot lattice transport measurements
David M. A. Mackenzie, Alberto Cagliani, Lene Gammelgaard, Bjarke S. Jessen, Dirch H. Petersen, Peter Bøggild, and Timothy J. Booth.
Int. J. Nanotechnol, accepted, (2016), Ref. [127]

The hot pick-up technique for batch assembly of van der Waals heterostructures
Filippo Pizzocchero, Lene Gammelgaard, Bjarke S. Jessen, José M. Caridad, Lei Wang, James Hone, Peter Bøggild, and Timothy J. Booth.
Nature Communications (2016), Ref. [20]

Graphene transport properties upon exposure to PMMA processing and heat treatments
Lene Gammelgaard, José M. Caridad, Alberto Cagliani, David M. A. Mackenzie, Dirch H. Petersen, Timothy J. Booth, and Peter Bøggild.
2D Materials (2014), Ref. [46]

Conference Contributions

Graphene antidot lattice transport measurements
David M. A. Mackenzie, Alberto Cagliani, Lene Gammelgaard, Bjarke S. Jessen, Dirch H. Petersen, and Peter Bøggild.
AMN-7 (2015)

Influence of individual process steps on graphene device characteristics
Lene Gammelgaard, Erol Zekovic, David M. A. Mackenzie, Jose M. Caridad, Alberto Cagliani, Timothy J. Booth and Peter Bøggild.
Graphene 2014 (2014)

Towards few-row graphene antidot lattice transistors
Bjarke S. Jessen, Alberto Cagliani, David M. A. Mackenzie, Lene Gammelgaard, and Peter Bøggild.
Carbonhagen 2013 (2013)

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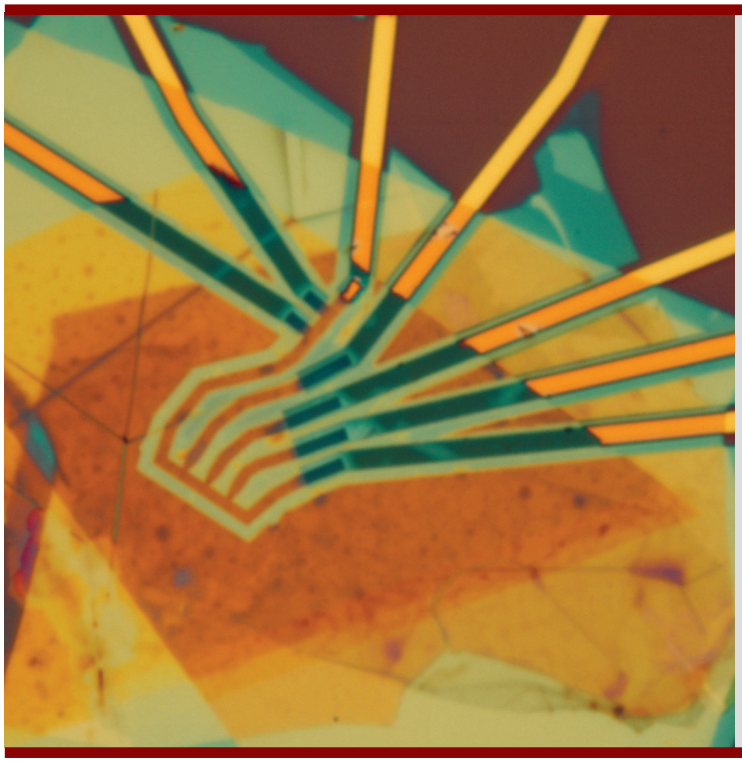

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